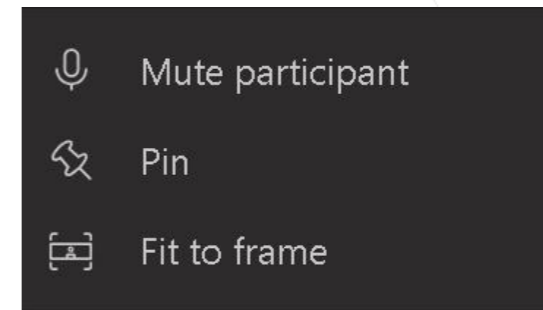


LAB

Simulation
of Proximity Lithography

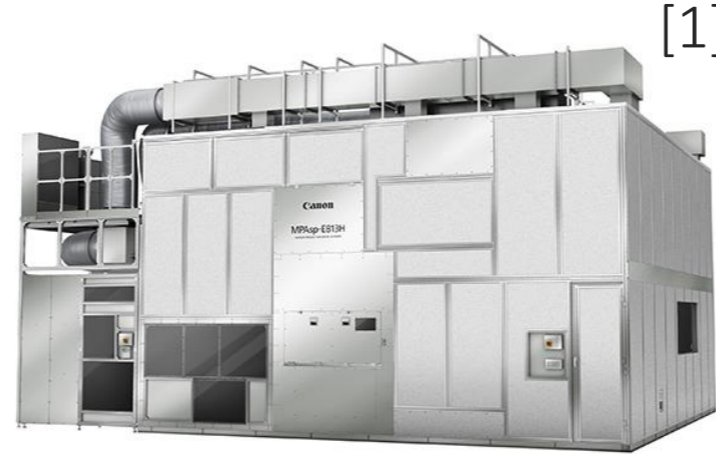
- **IMPORTANT NOTICE:** Please note that this session will be recorded. By joining these webinar sessions, you automatically consent to such recordings. If you do not consent to being recorded, do not join the session.
 - Q&A will not be recorded
- MS Teams essentials (App Users):
 - Right click on image, use „Pin“ to enlarge
- This webinar is an overview / introduction to proximity lithography simulation
 - It picks out essential ingredients, focus on applications cases from the field.
 - In case you want / need more depth -> Contact support@genisys-gmbh.com



- Proximity Lithography
- 3D Exposure Simulation
- Application Cases
 - Proximity Artifacts Tracking
 - Sidewall Angle Optimization
 - Greyscale Lithography
 - Topography Simulation
 - Resolution Enhancement
- Summary

Proximity Lithography Applications

- Mask Aligner



- Flat Panel Displays



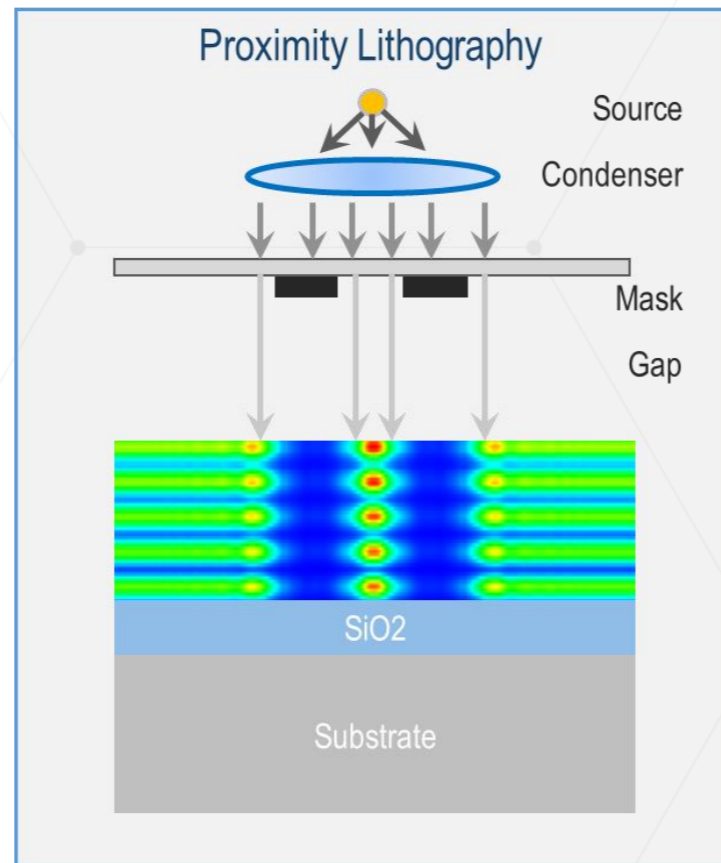
- Micro-Electro-Mechanical System (MEMS)



- Chip-Backend & Packaging

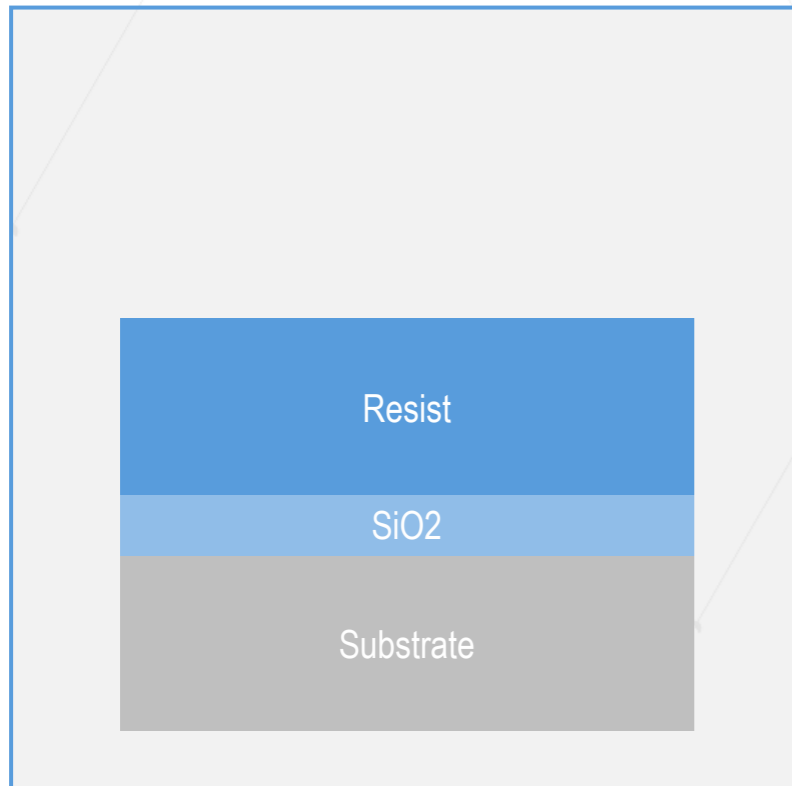


- Proximity lithography is an important photolithography technique for manufacturing integrated circuit and MEMS Systems.
- Schematic view of proximity lithography:

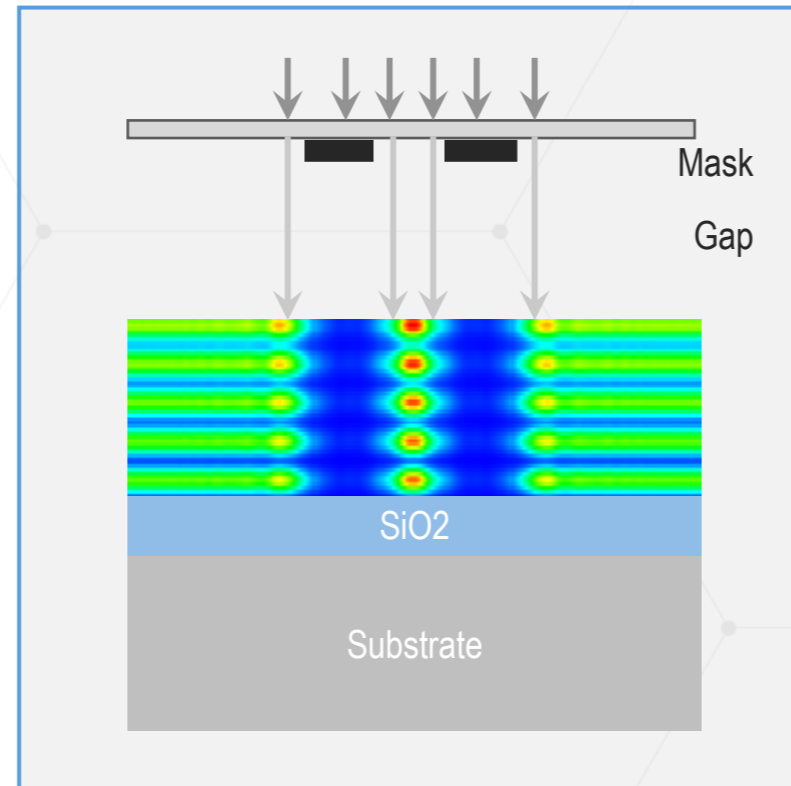


- Proximity lithography = „Shadow Printing“

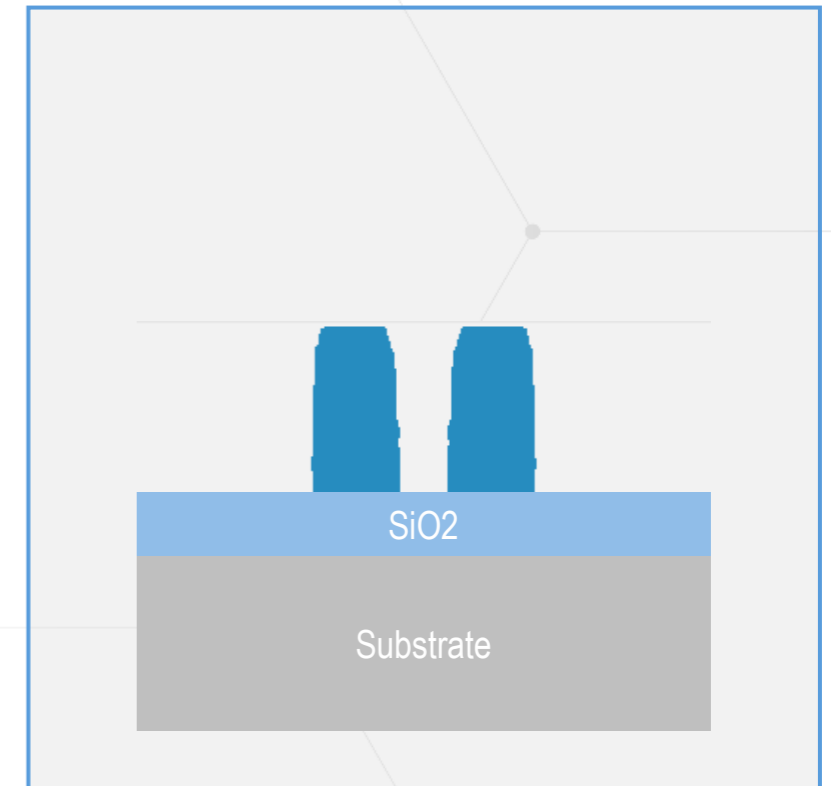
Wafer preparation



Optical exposure

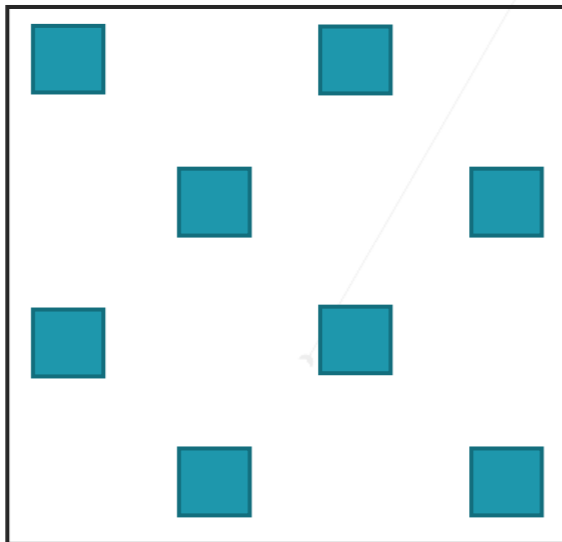


Resist development

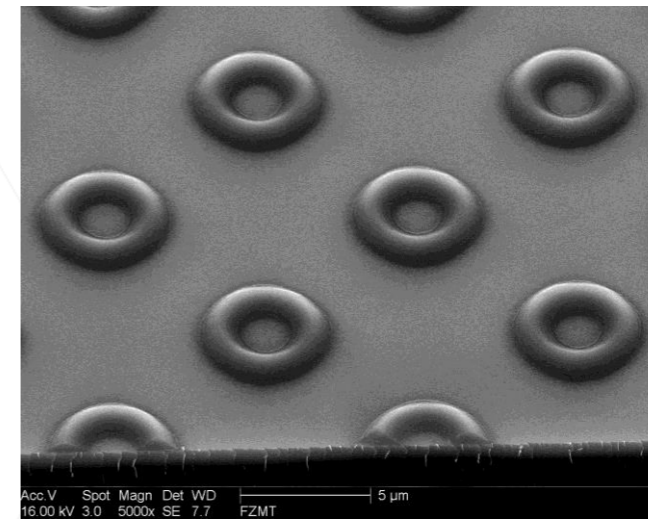


- However, pattern fidelity is an issue with decreasing feature size and increasing proximity gap.
 - Example: 3 μm squares exposed with 20 μm proximity gap on 2 μm AZ6624/Si substrate

Mask layout

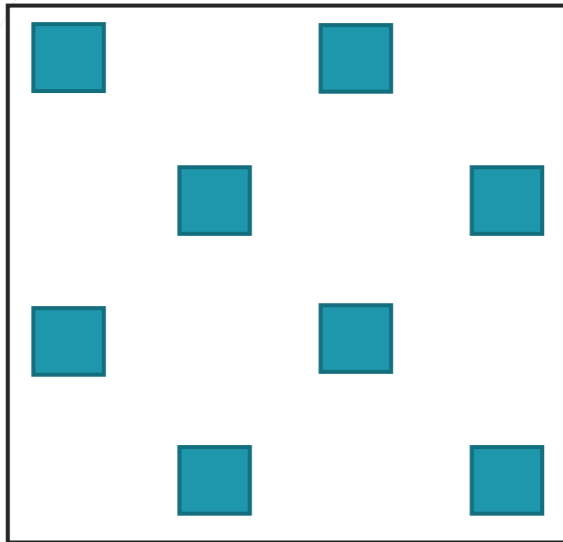


SEM image



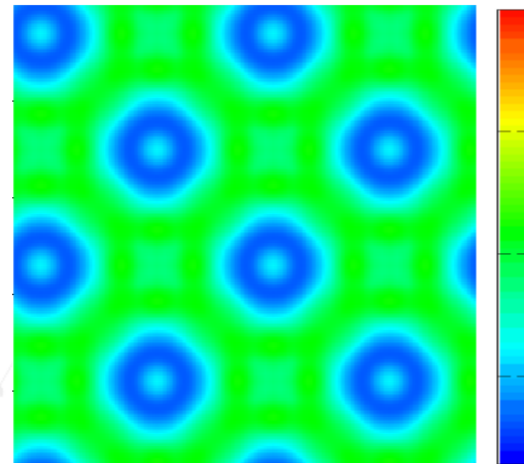
- How can the issue be understood?
- Pre-exposure simulation and analysis is cost and time effective for proximity lithography.

Mask layout

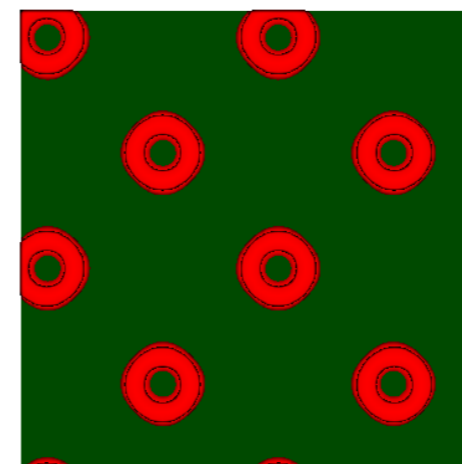


Simulation

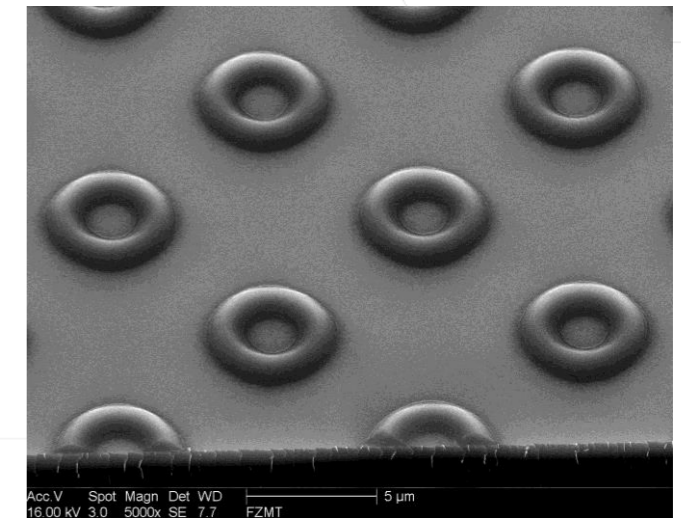
Bulk image



Resist profile

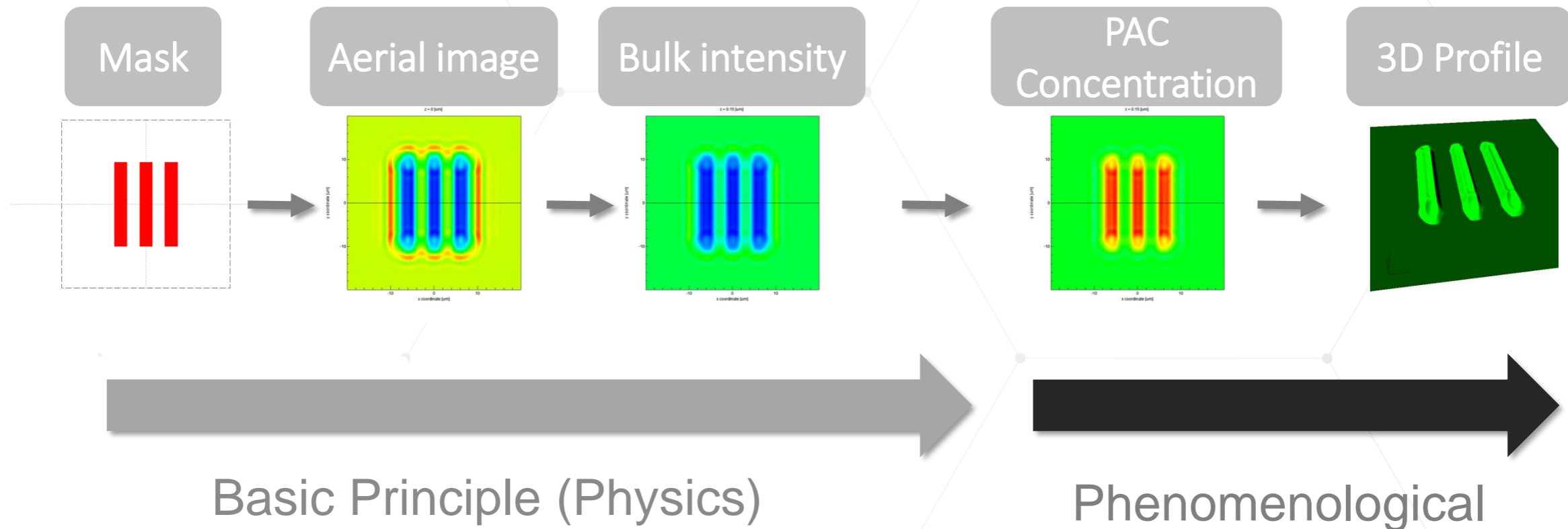


SEM image

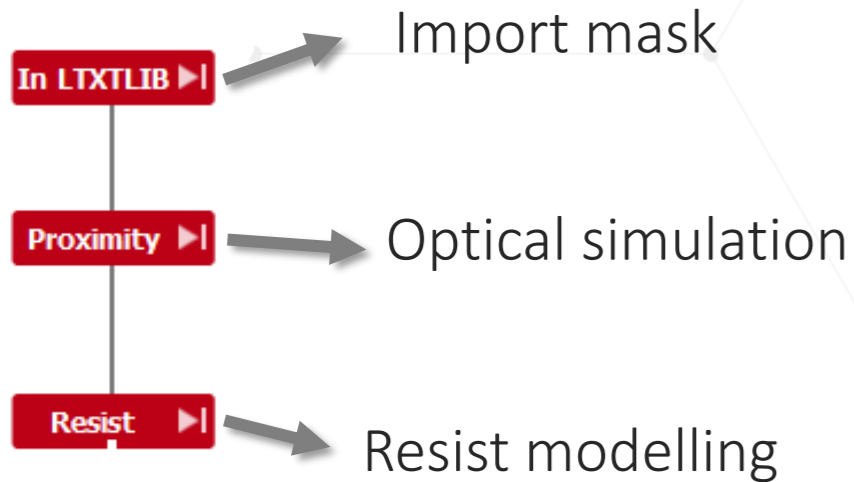


- Proximity Lithography
- 3D Exposure Simulation
- Application Cases
 - Proximity Artifacts Tracking
 - Sidewall Angle Optimization
 - Greyscale Lithography
 - Topography Simulation
 - Resolution Enhancement
- Summary
- Q&A

- LAB allows full simulation of proximity lithography, including bulk intensity and 3D resist profile.
- In most cases, bulk intensity is enough for exposure analysis.

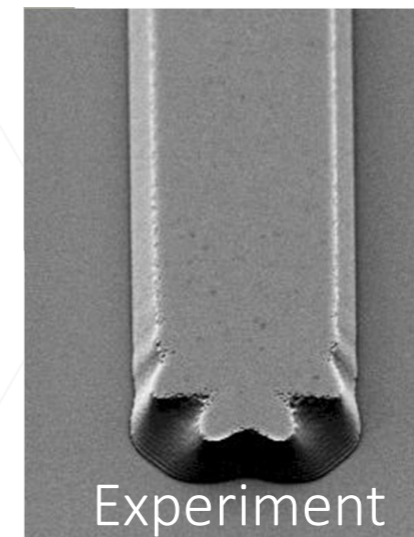
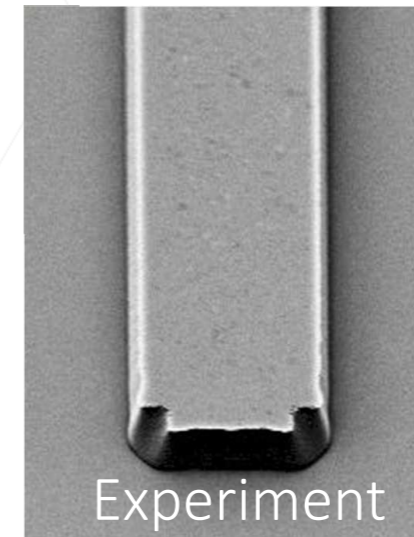


- LAB simulation flow:



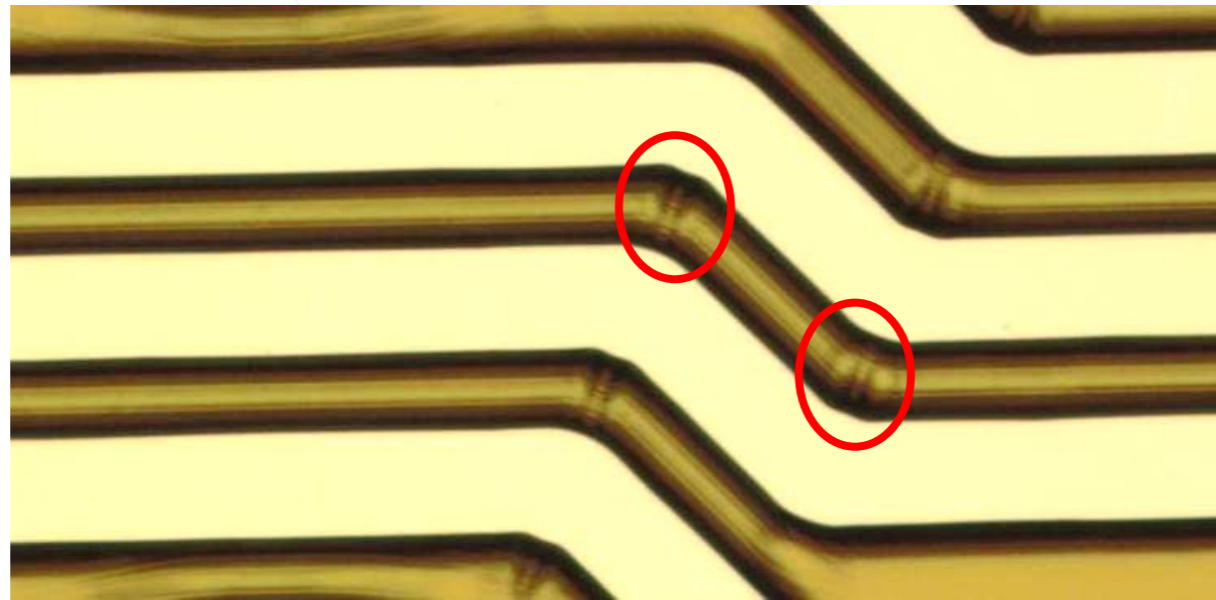
- With a proper setup, simulation can predict the resist shape with high accuracy[5].

3D resist experiment vs simulation for two different sources



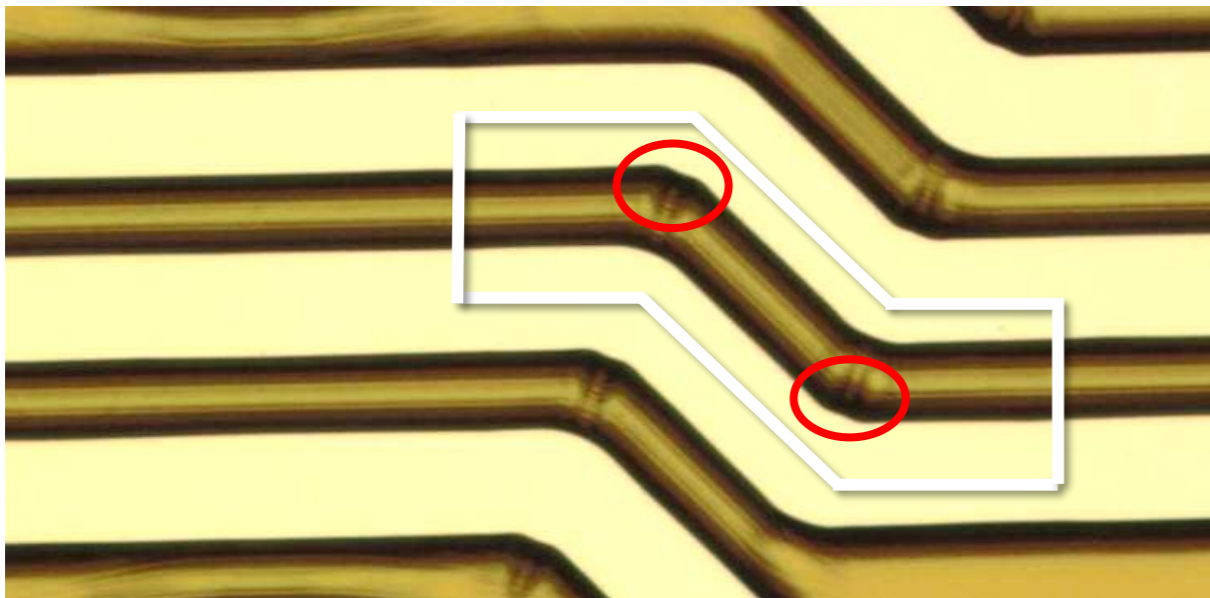
- Proximity Lithography
- 3D Exposure Simulation
- Application Cases
 - Proximity Artifacts Tracking
 - Sidewall Angle Optimization
 - Greyscale Lithography
 - Topography Simulation
 - Resolution Enhancement
- Summary
- Q&A

- Proximity artifacts are prominent at positions where the symmetry of structures are broken.
- The example below is an optical microscopy image of resist structure, acting as an etch mask. The artifacts will induce unwanted deformations in the etched layer[6].

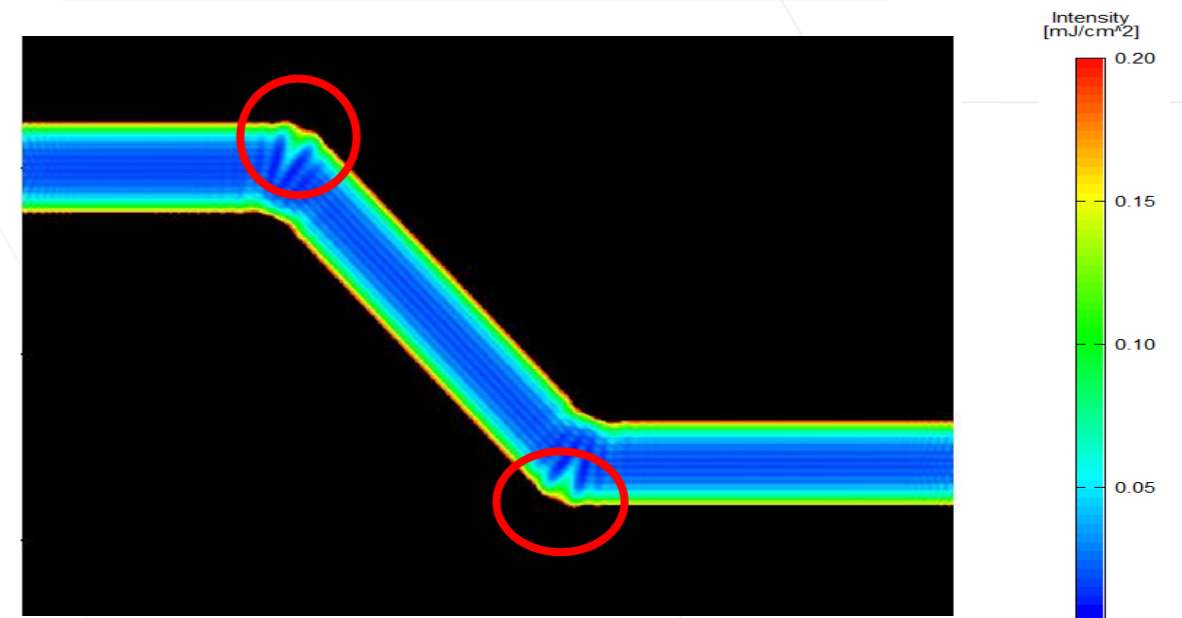


- How to avoid the artifacts with the help of simulation?
- The first step is to reproduce the proximity artifacts via simulation.

Optical microscopy image of resist structure



Intensity image from simulation



- Optimization is carried out to avoid the artifacts completely and improve process stability.
- LAB simulation has the access to
 - exposure parameters (dose, gap, source)
 - pattern parameters (line width, fillet radius at the corner)

shape dependence

shape_dependence_arti..

Mapping

Proximity (1)

gap dependence

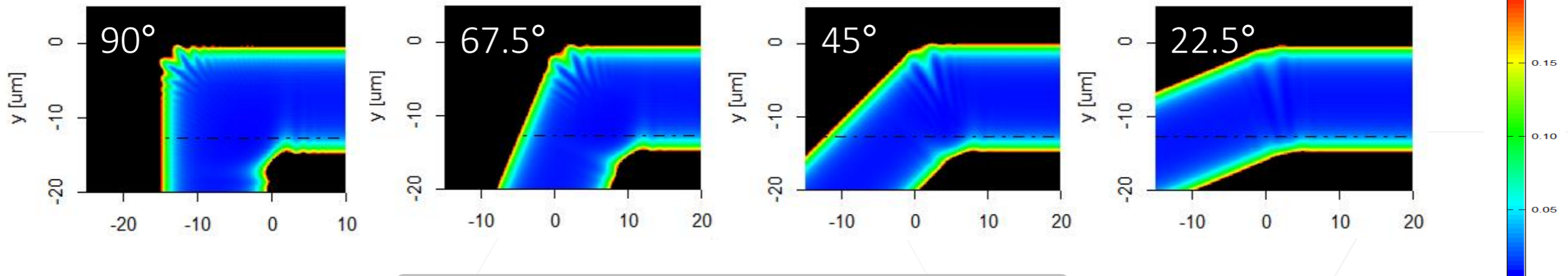
angle90

gap 20um

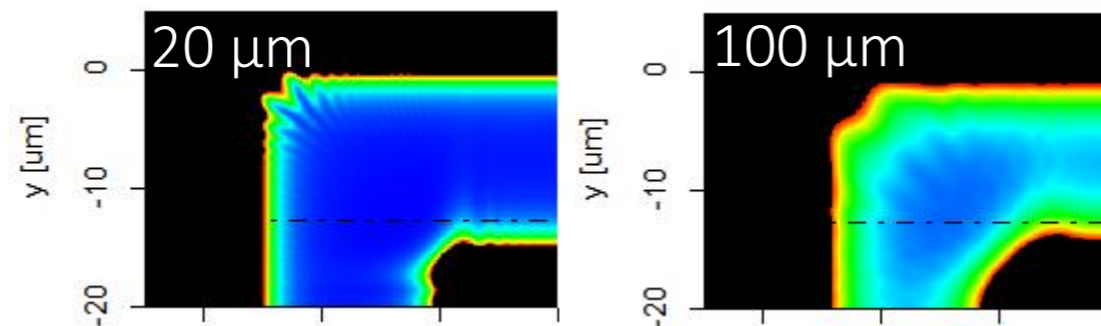
gap 100um

- Dependence of artifacts on corner angle and exposure gap
 - Proximity artifacts may be avoided by decreasing the corner angle or increase exposure gap.

Intensity image for varied corner angle



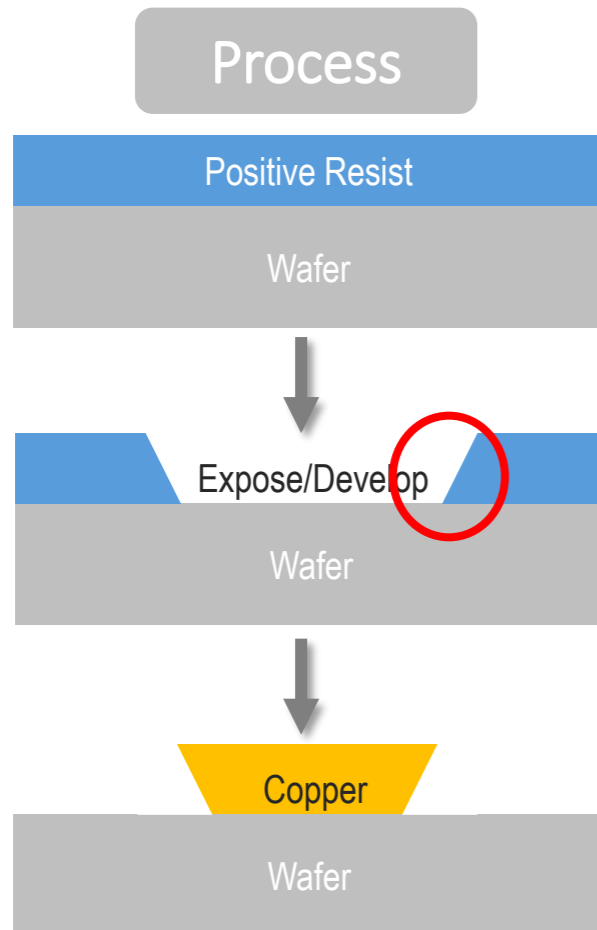
Intensity image for varied proximity gap



- Proximity Lithography
- 3D Exposure Simulation
- Application Cases
 - Proximity Artifacts Tracking
 - Sidewall Angle Optimization
 - Greyscale Lithography
 - Topography Simulation
 - Resolution Enhancement
- Summary
- Q&A

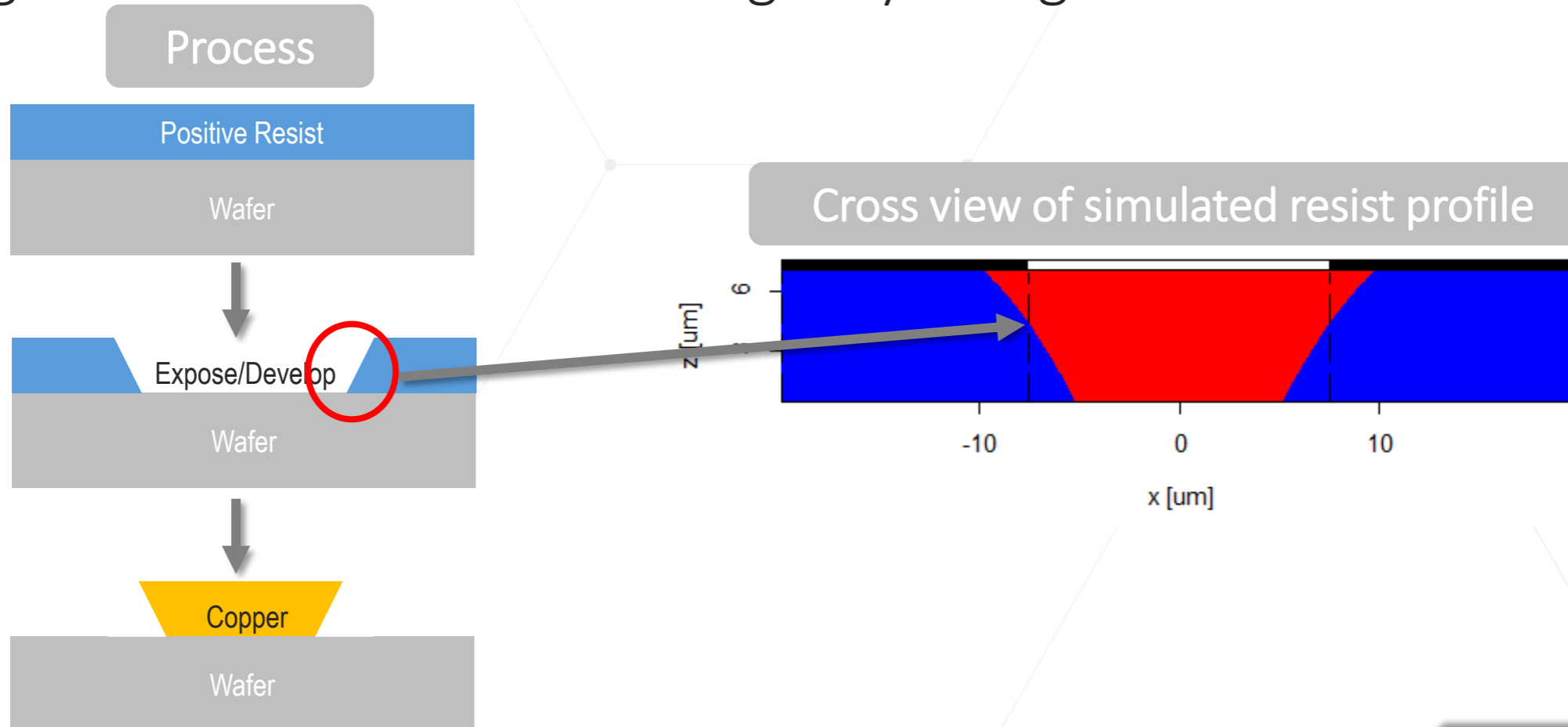
Simulation for Sidewall Angle

- In a copper plating process, the copper sidewall angle is controlled by the resist sidewall.

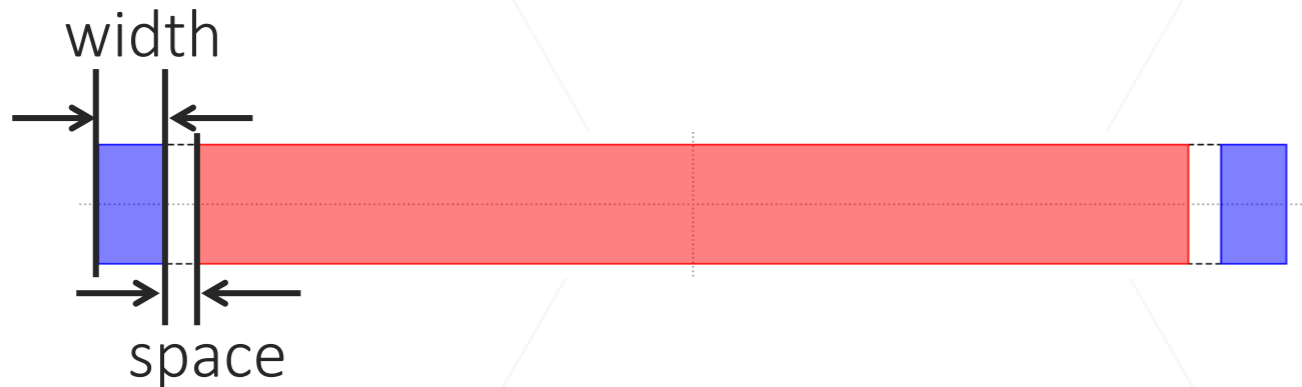


Simulation for Sidewall Angle

- In a copper plating process, the copper sidewall angle is controlled by the resist sidewall.
- The resist sidewall angle is available in LAB simulation.
- Target: increase the sidewall angle by 7 degree



- How to optimize the sidewall angle?
 - Both optical source and pattern can be optimized.
 - A simple optical proximity correction (OPC) pattern with a sidebar is proposed for sidewall angle increase.

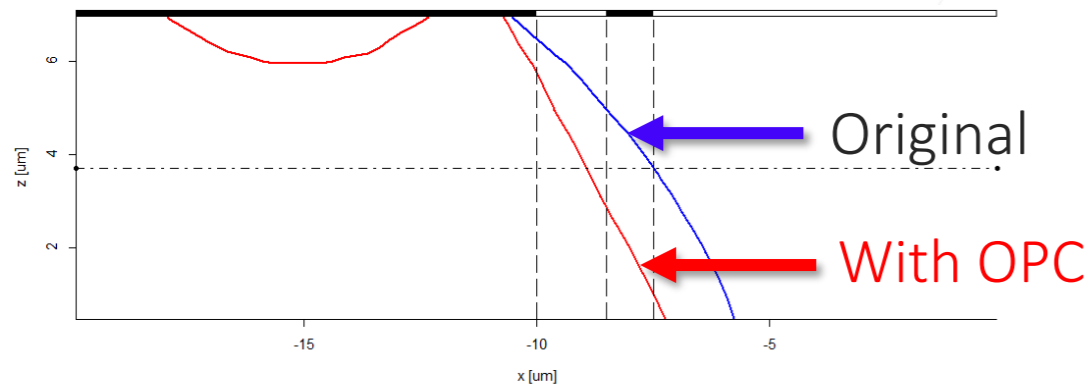


- Both the width and the space of the sidebar can be optimized.
 - With the demo flow, the sidewall angle is optimized with a loop module.

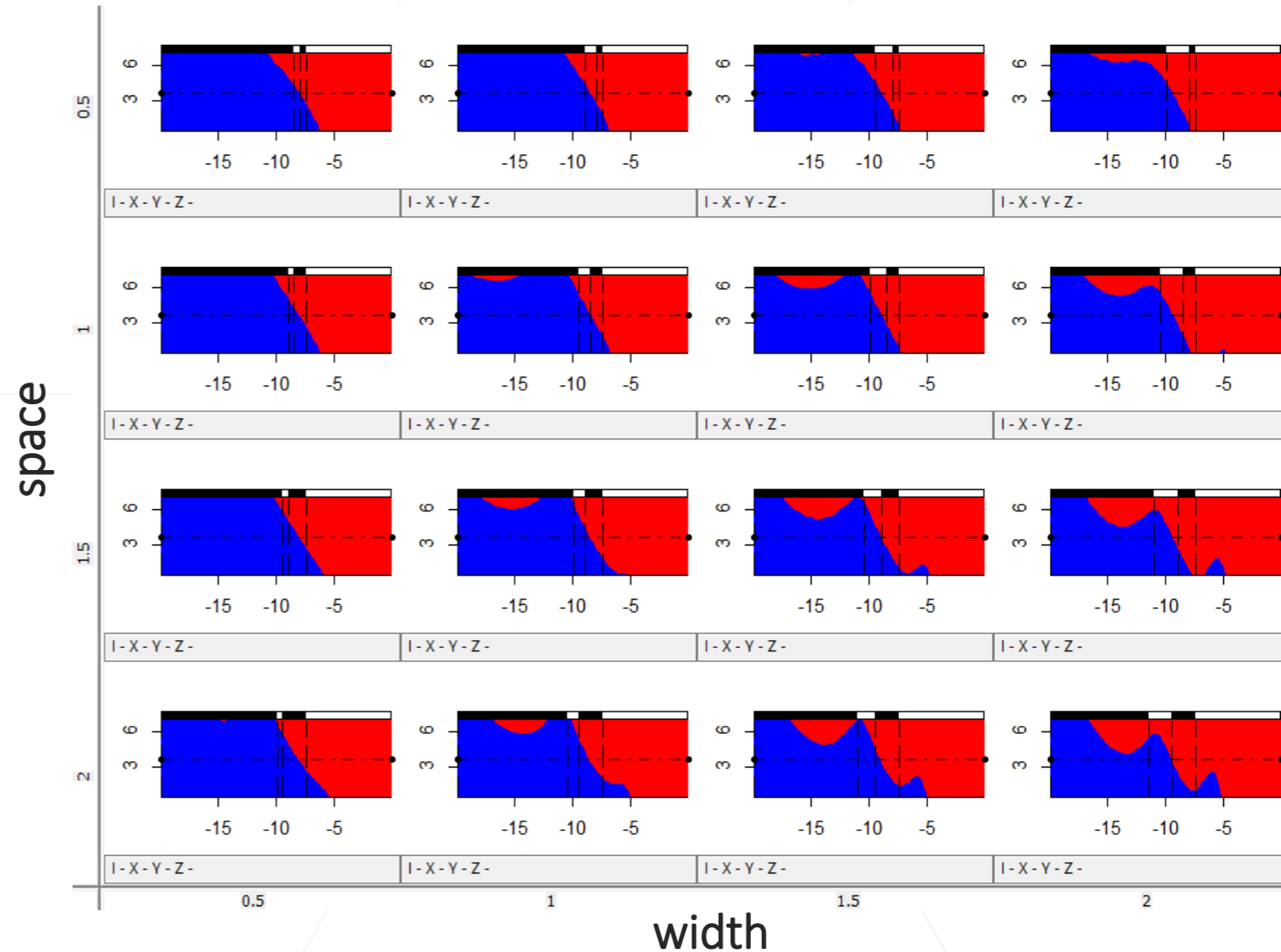
Sidewall Angle Optimization

- Optimization of the sidebar:
 - With width = 1.5 μm , space = 1 μm , the sidewall angle is increased by 8 degree.

Cross view overlap



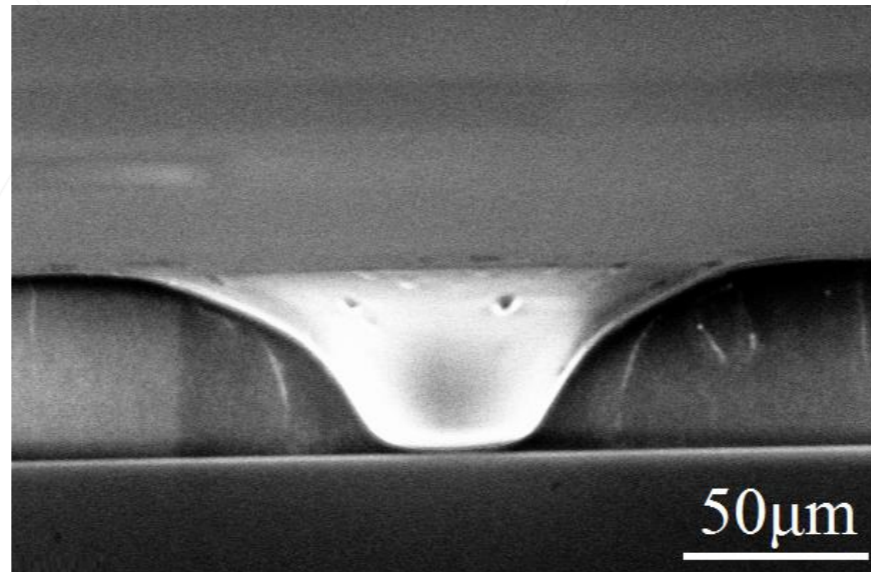
Cross view of simulated edge profile



- Proximity Lithography
- 3D Exposure Simulation
- Application Cases
 - Proximity Artifacts Tracking
 - Sidewall Angle Optimization
 - Greyscale Lithography
 - Topography Simulation
 - Resolution Enhancement
- Summary
- Q&A

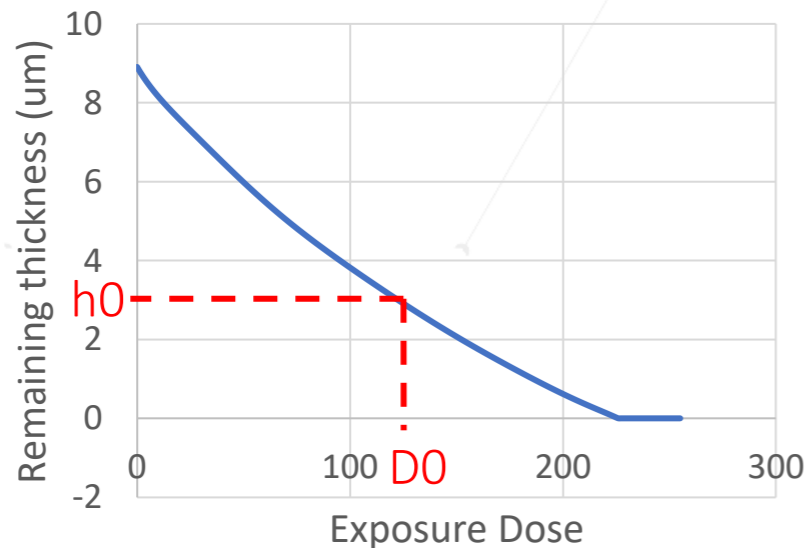
- Greyscale (depth variation) structure has considerable benefit to MEMS technologies.
 - Example: fabricating a tapered sidewall aperture with feature height of 50 μm [7].

Cross section of the aperture with a tapered sidewall extending over 240 μm

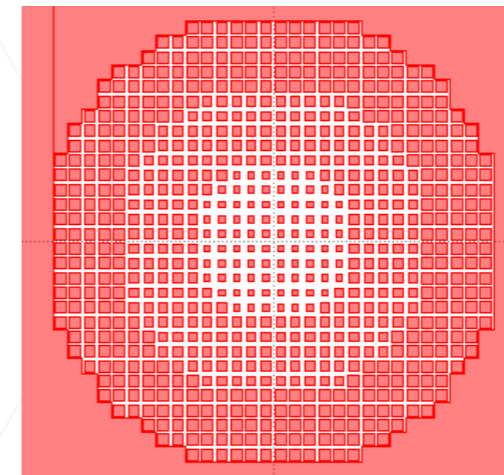


- Greyscale lithography works well with a large variety of low contrast photoresist, e.g. AZ9260.
- To achieve desired depth, the corresponding dose is tuned by the pattern density. The pattern is subwavelength scale to avoid unwanted diffraction.
- Moreover, the resist shape is affected by lateral development.

Contrast curve

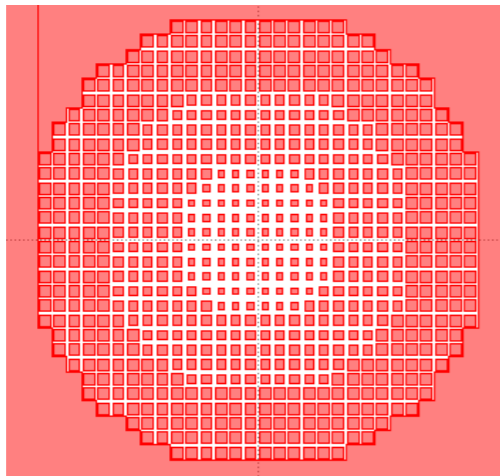


Designed pattern

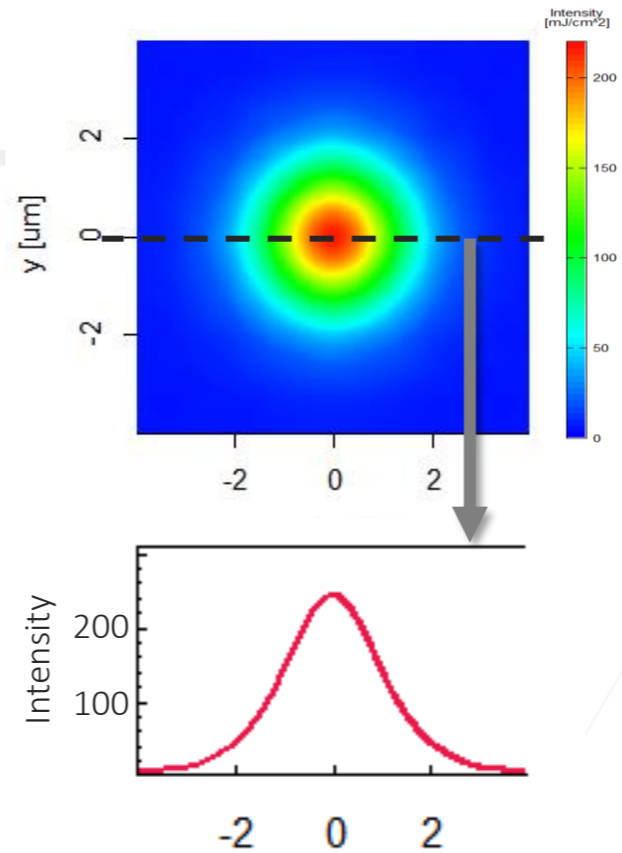


- LAB models the resist shape by taking into account the resist development process.

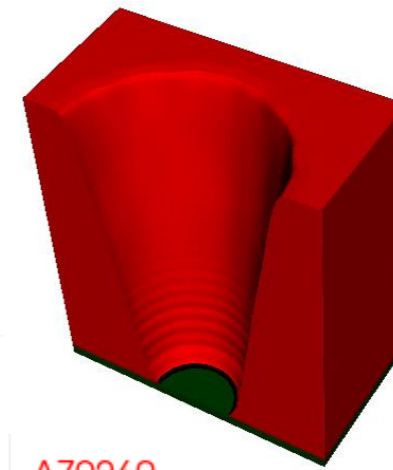
Designed pattern



Calculated intensity



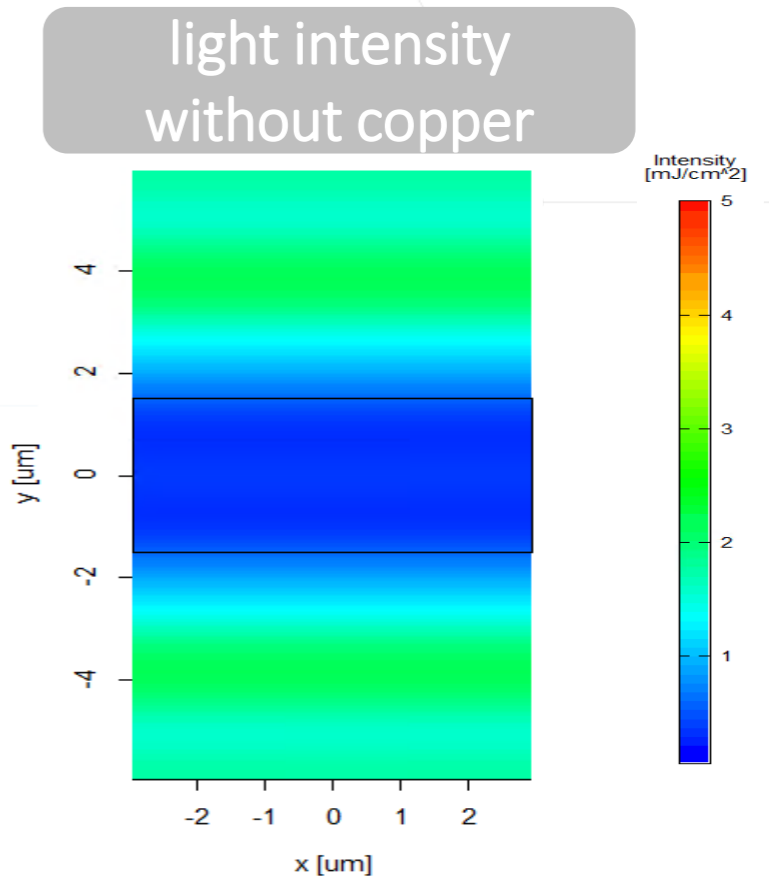
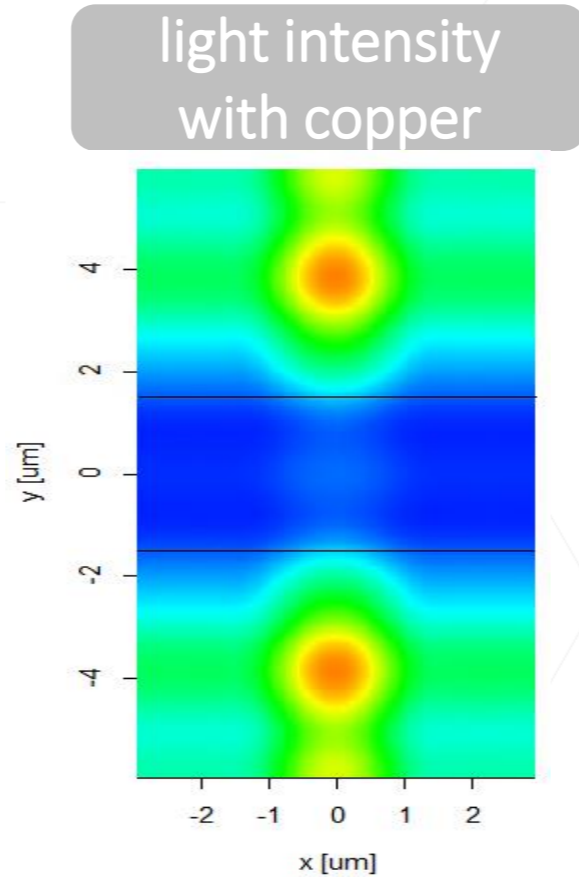
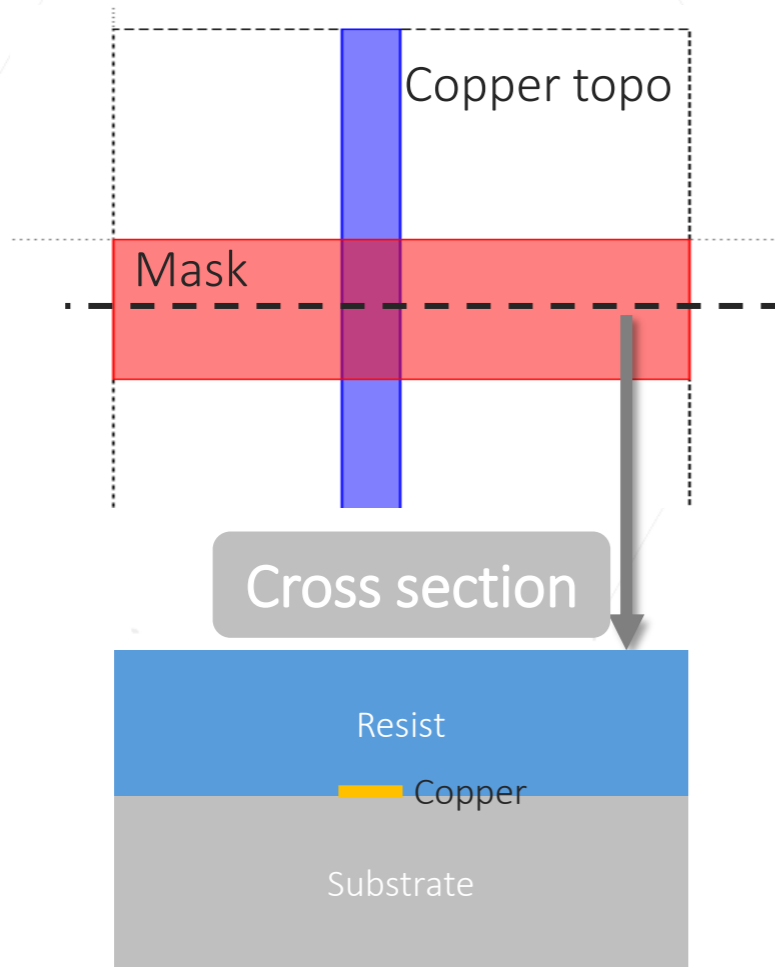
Calculated profile



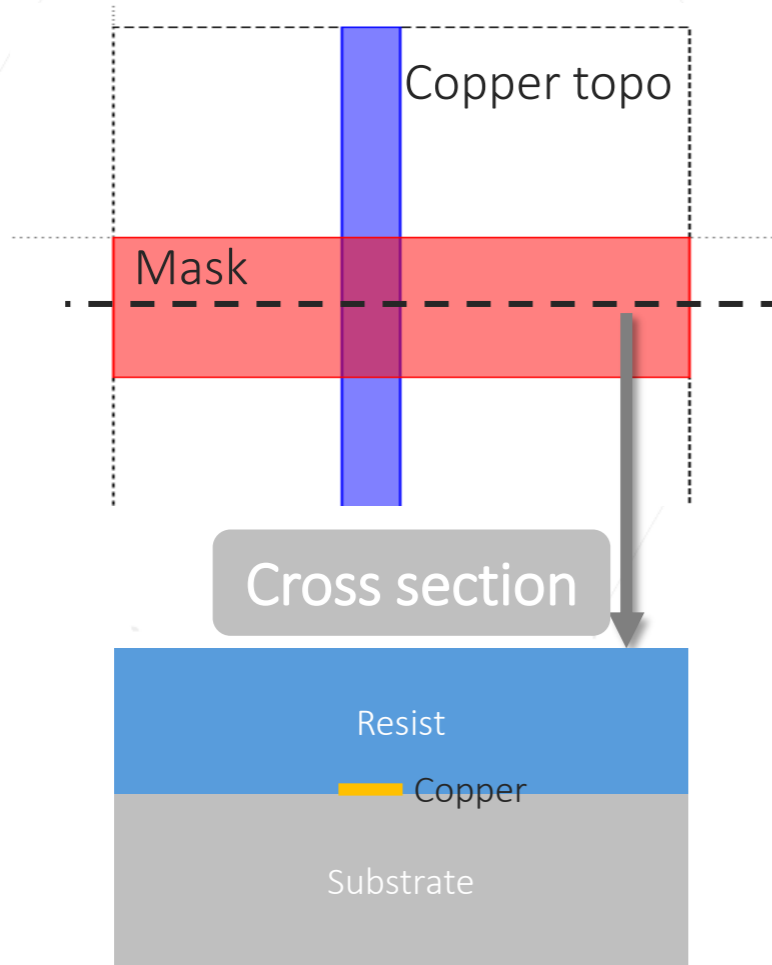
AZ9260
SiO2

- Proximity Lithography
- 3D Exposure Simulation
- Application Cases
 - Proximity Artifacts Tracking
 - Sidewall Angle Optimization
 - Greyscale Lithography
 - Topography Simulation
 - Resolution Enhancement
- Summary
- Q&A

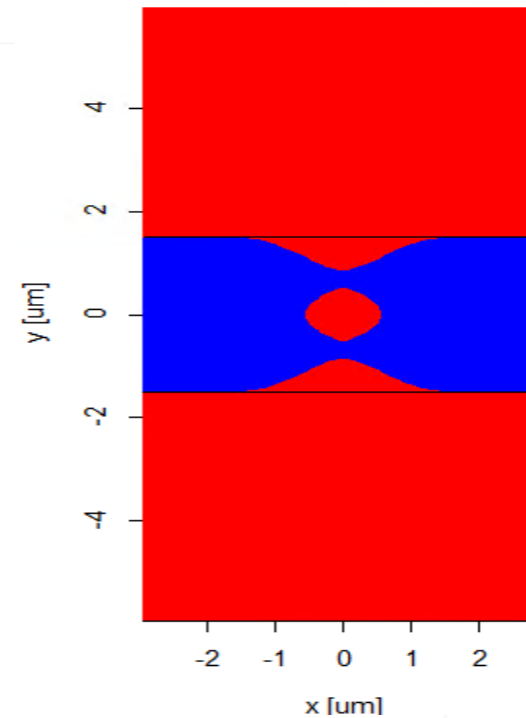
- Topography simulation is to calculate the influence of non-flat substrate.
- The example shows the modification of intensity distribution resulting from strong reflection of the thin copper layer.



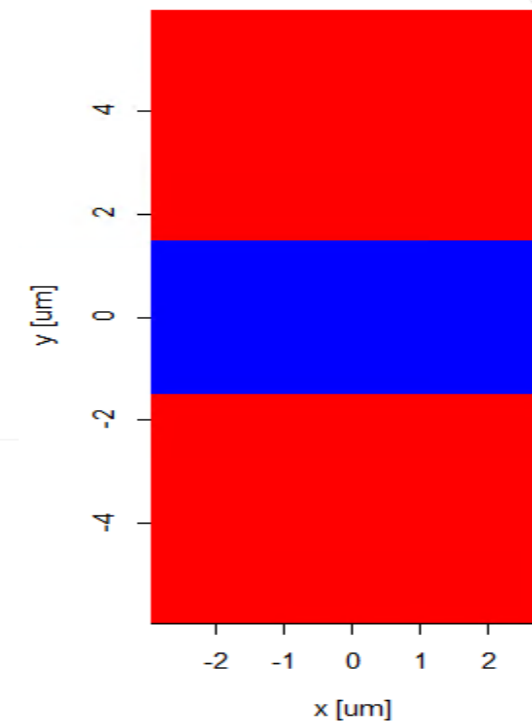
- Topography simulation is to calculate the influence of pre-structured substrate.



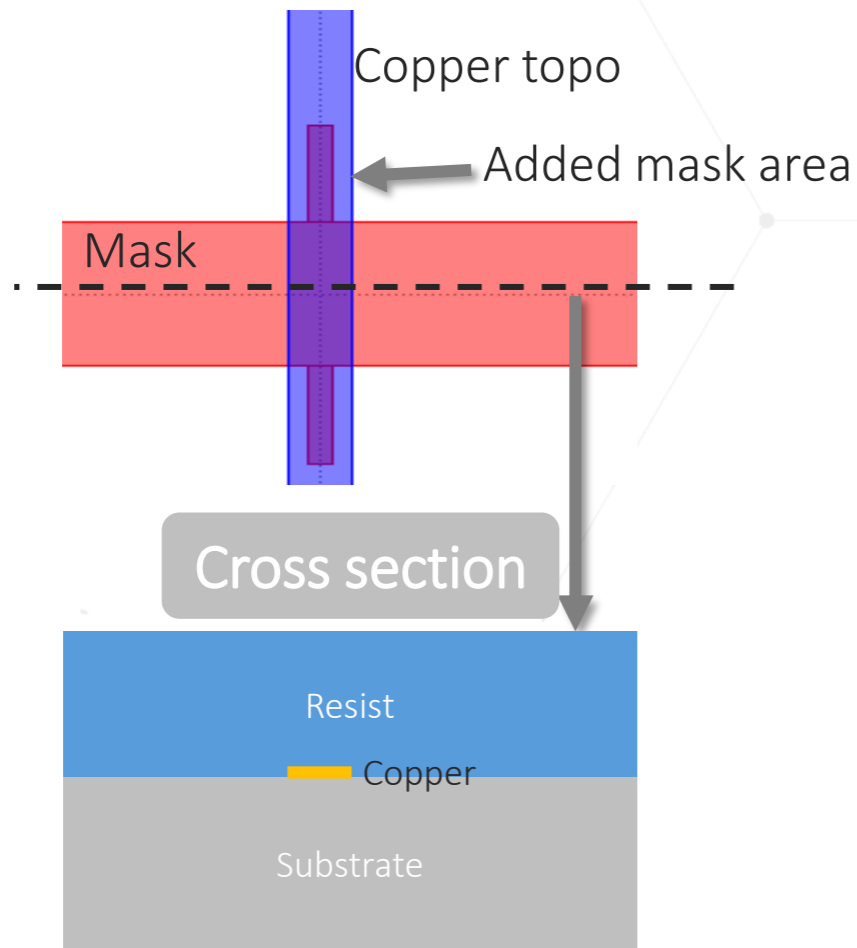
Resist profile with copper



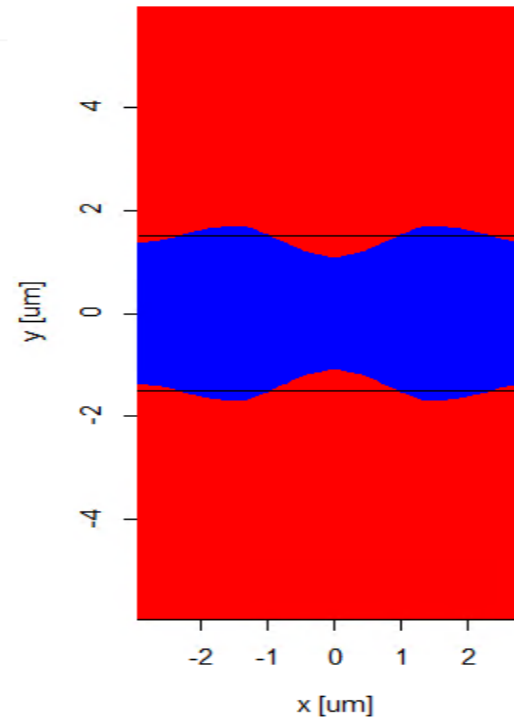
Resist profile without copper



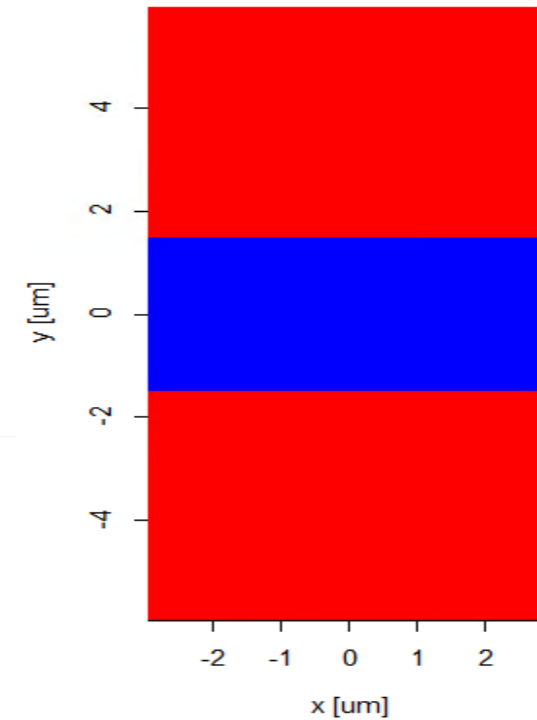
- To compensate the unexpected exposure at the line center, the mask is modified with the added mask area.



Resist profile with copper



Resist profile without copper



- Proximity Lithography
- 3D Exposure Simulation
- Application Cases
 - Proximity Artifacts Tracking
 - Sidewall Angle Optimization
 - Greyscale Lithography
 - Topography Simulation
 - Resolution Enhancement
- Summary
- Q&A

- The resolution of proximity exposure is decreasing with proximity gap.
- A relatively large proximity gap is used in certain cases (e.g. flat panel display) to avoid issues, like mask contamination, resist sticking and mask damage.
- Application case:
 - Expecting a resolution of 4 μm at exposure gap 150 μm for general patterns.
 - First is to analyze the process feasibility for 4 μm patterns.

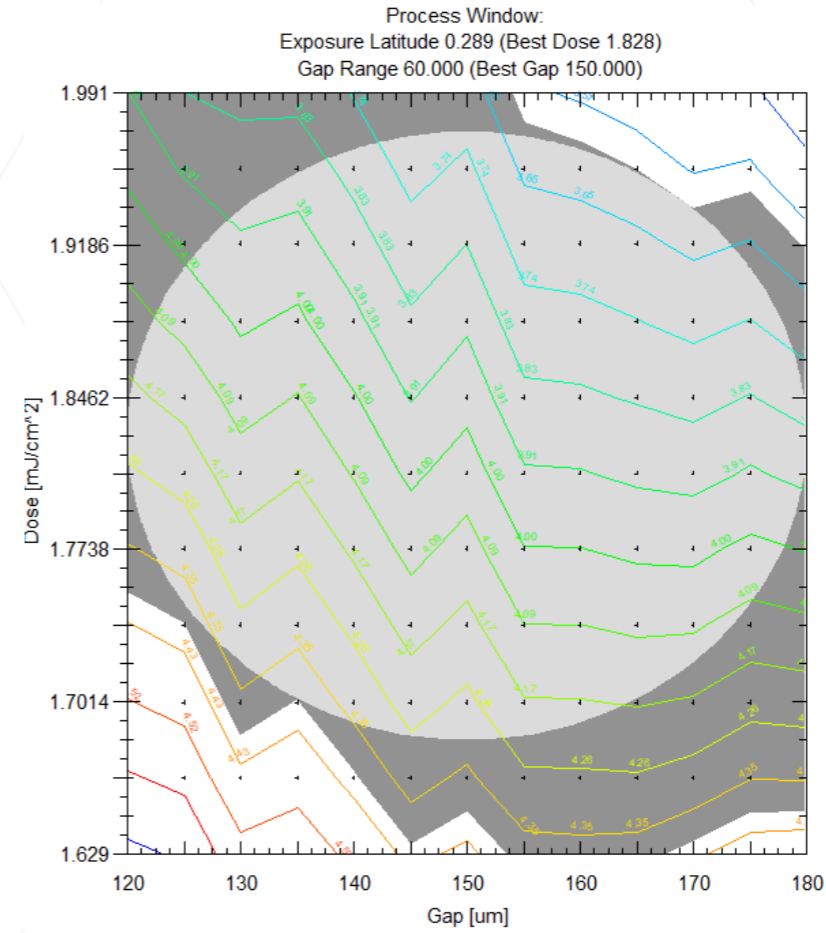
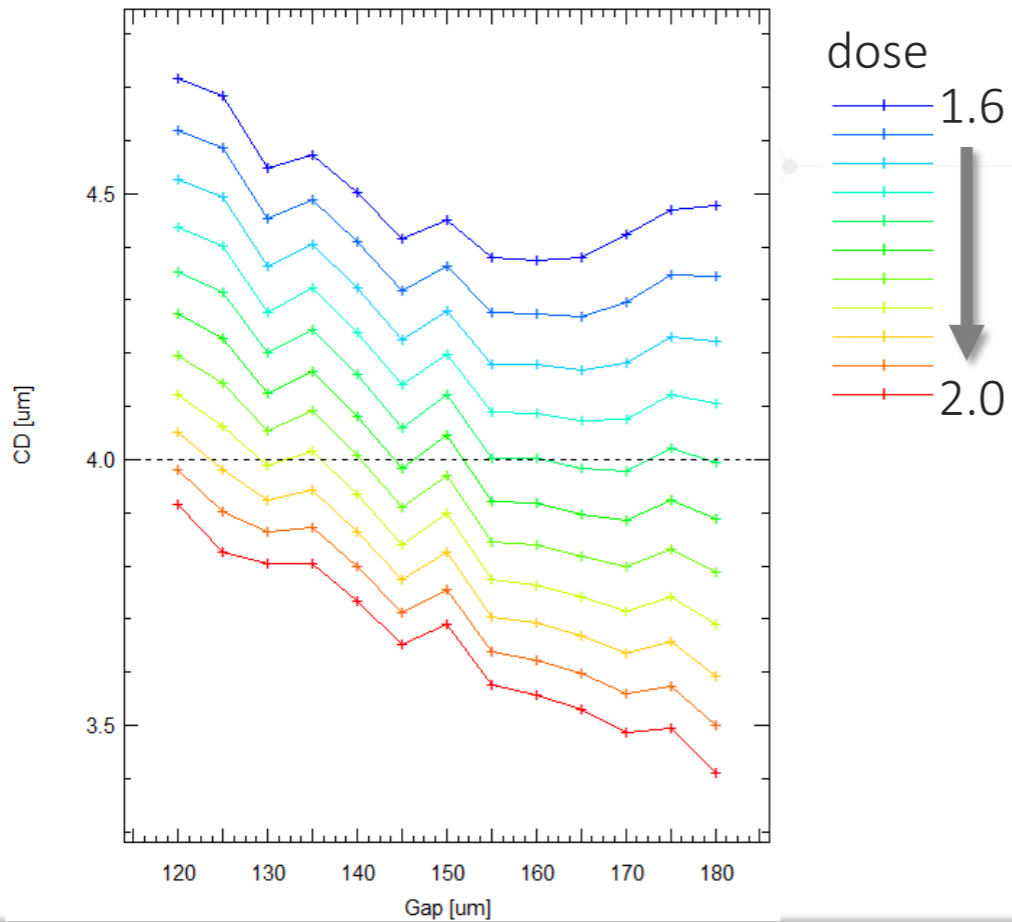


- Process feasibility verification for 4 μm line/space pattern
 - Dose-gap-matrix analysis models feature (CD, etc.) variation with dose and gap

Dose gap matrix analysis

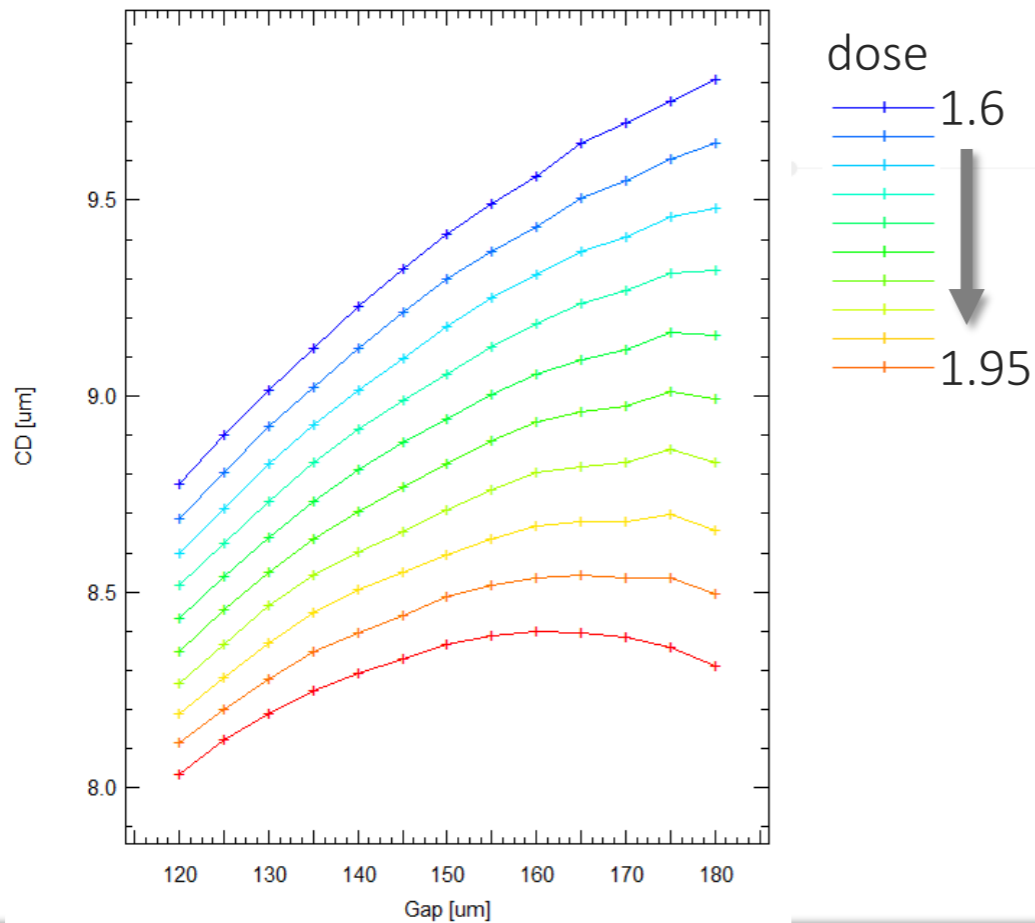


Process window

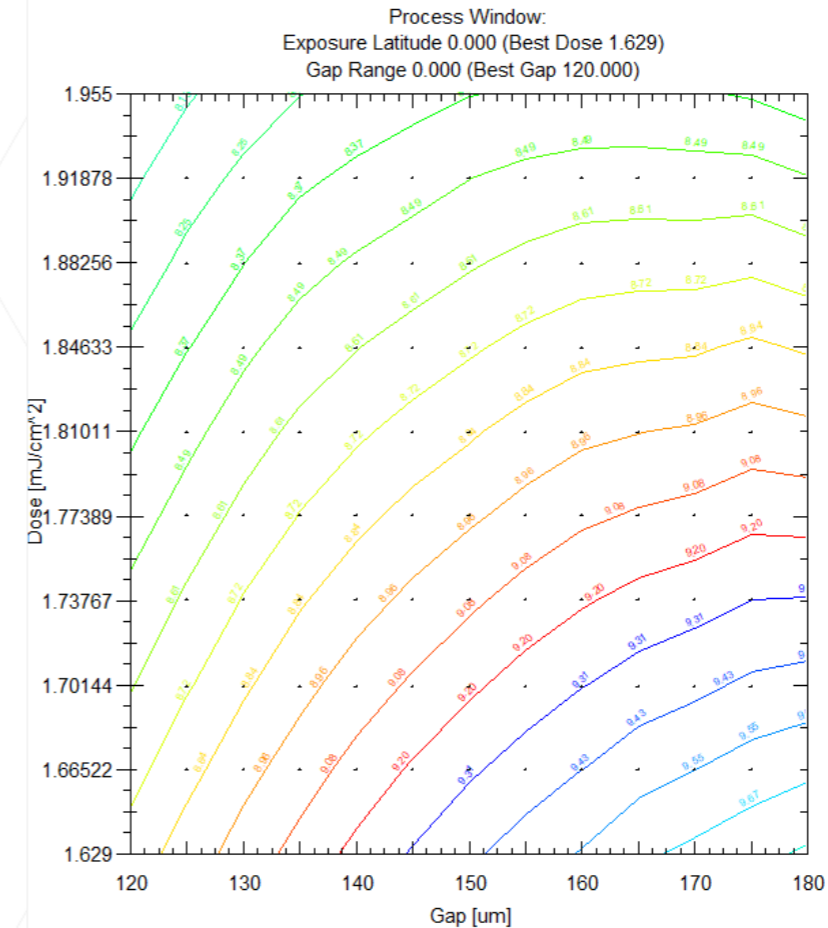


- Process feasibility verification for 4 μm isoline pattern
 - Dose-gap-matrix analysis verifies the process feasibility: not resolvable.

Dose gap matrix analysis

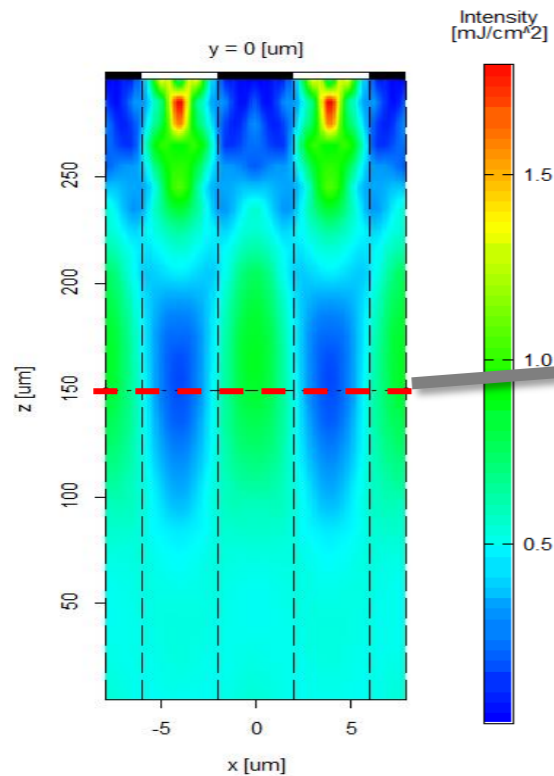


Process window

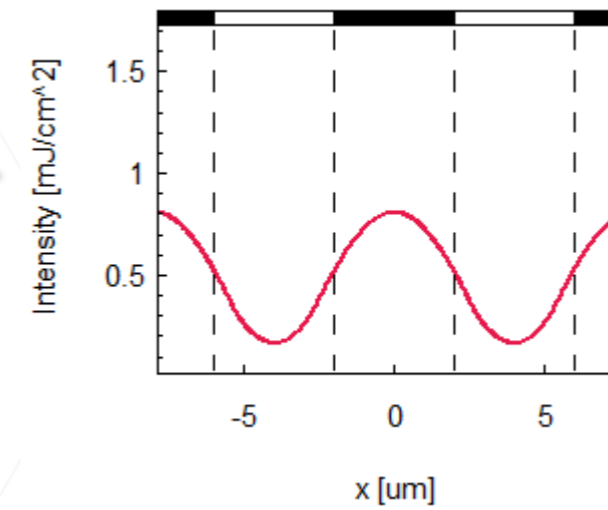


- Simulation in air presents the light diffraction after mask
 - 4 μm line/space pattern: Talbot effect

Diffraction after mask

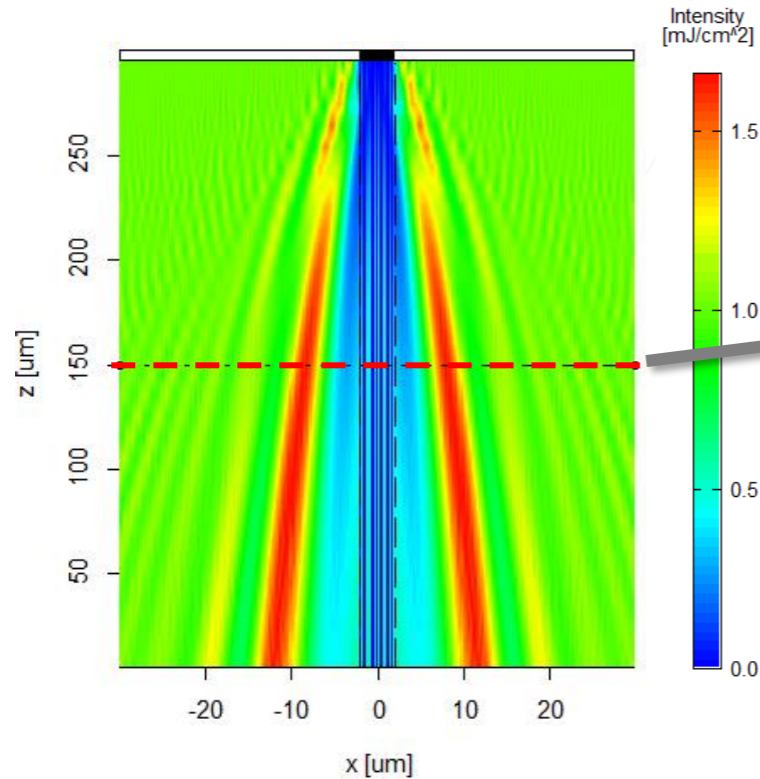


Aerial image @ 150 μm

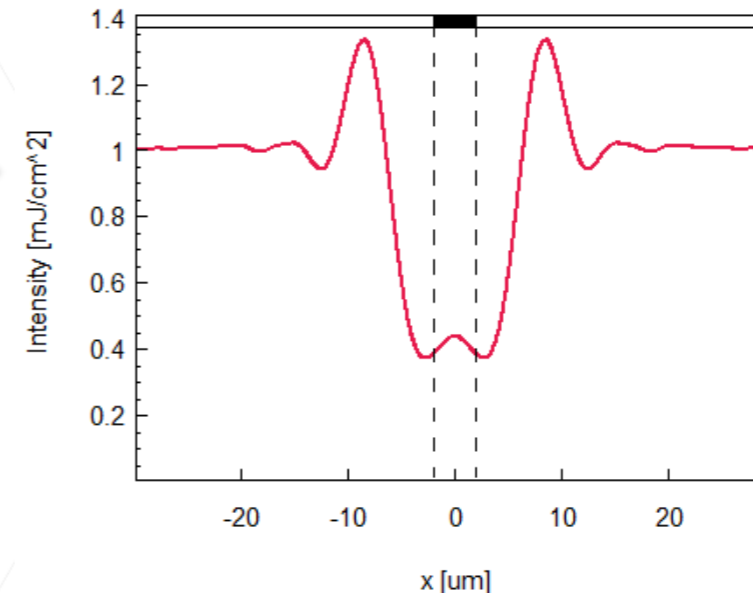


- Simulation in air presents the light diffraction after mask
 - 4 μm isoline pattern: feature is broadened

Diffraction after mask

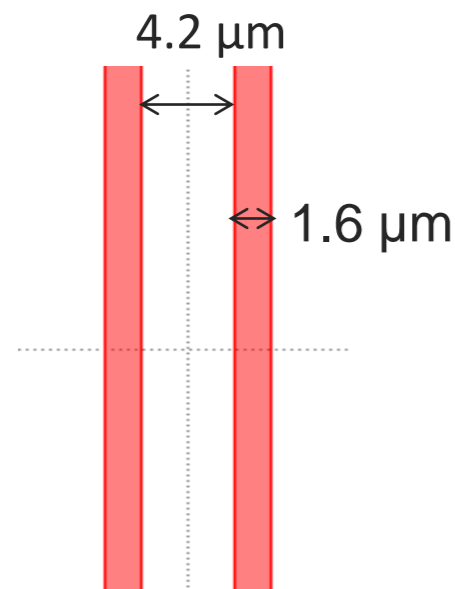


Aerial image @ 150 μm

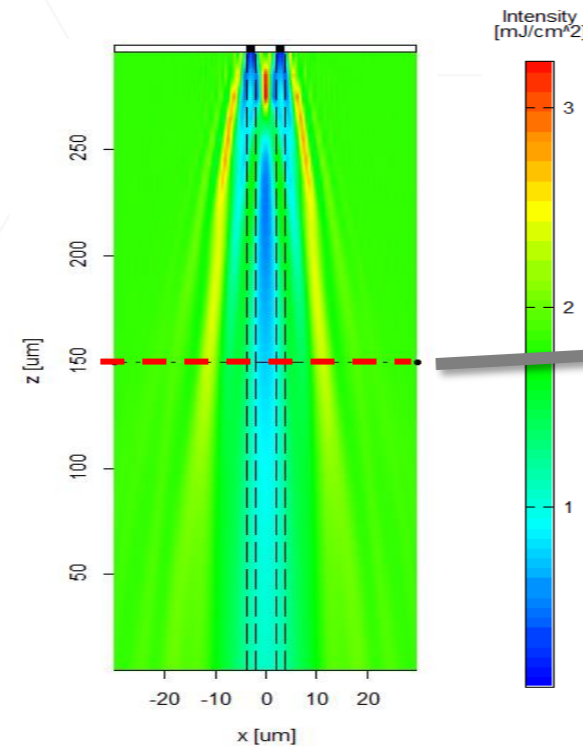


- The resolution can be enhanced by optical proximity correction (OPC).
 - The exposure condition is optimized for line/space pattern.
 - OPC is applied for 4 μm isoline.

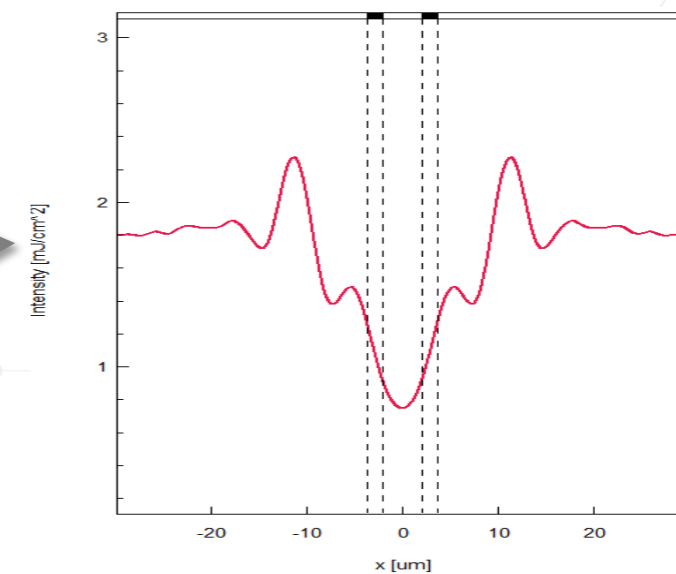
Isoline OPC



Diffraction after mask

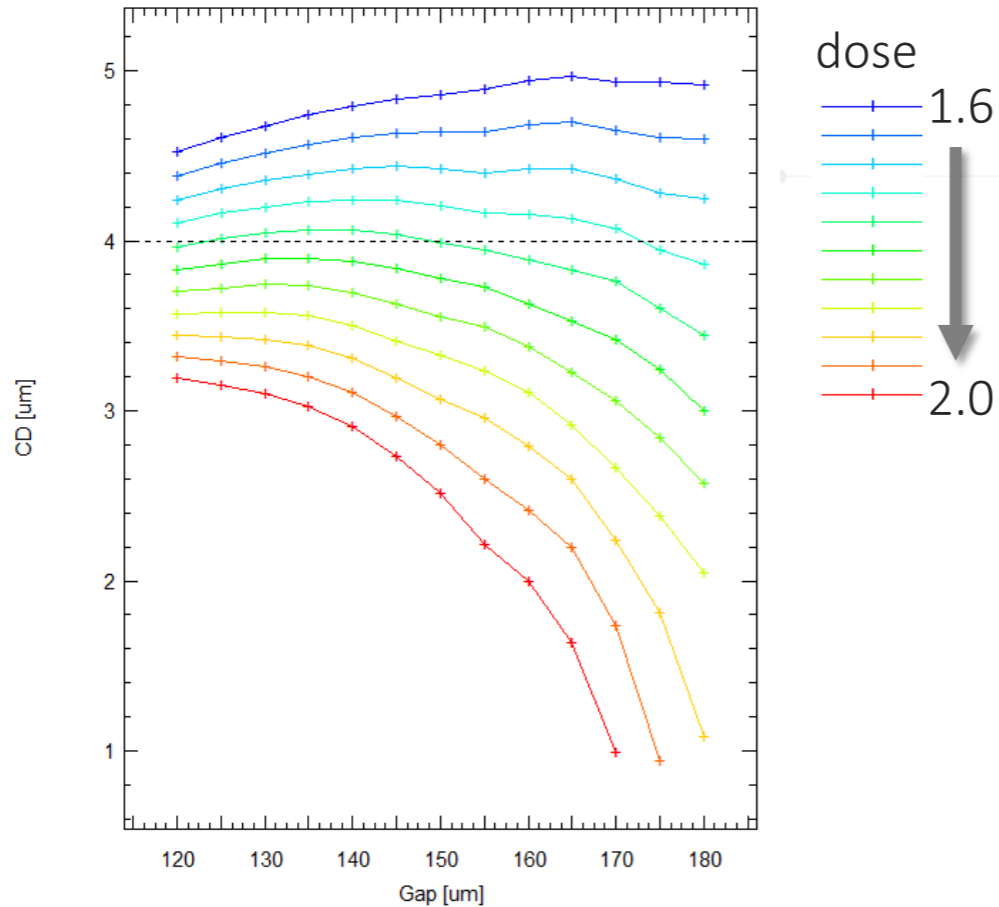


Aerial image @ 150 μm

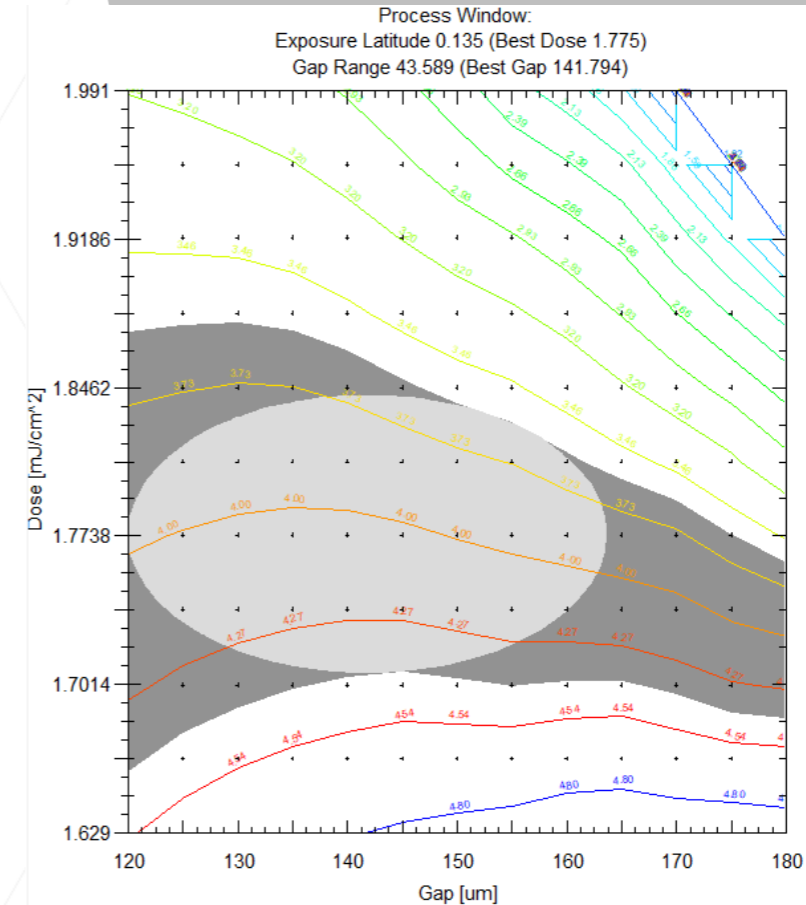


- The resolution is enhanced by optical proximity correction (OPC).
 - The exposure condition is optimized for line/space pattern.
 - OPC is applied for 4 μm isoline.

Dose gap matrix analysis

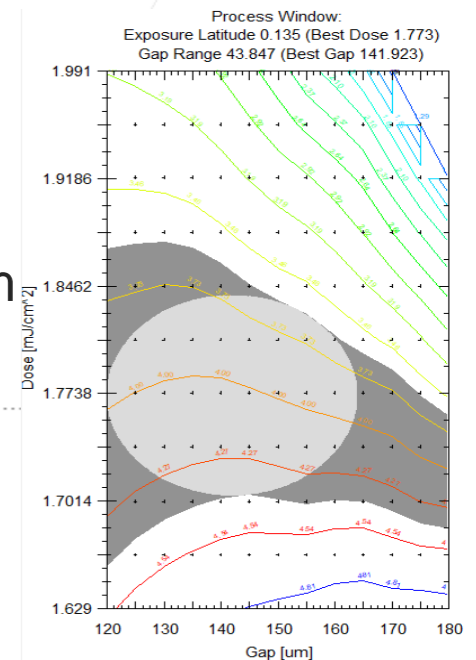
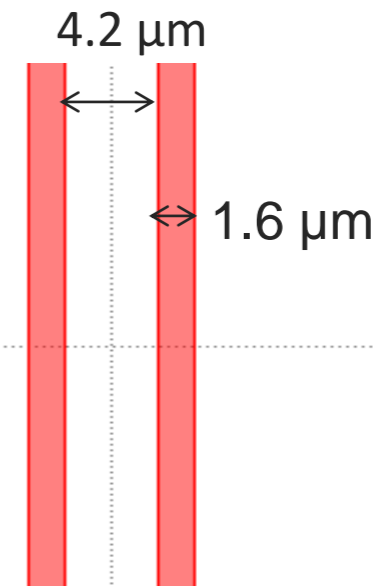
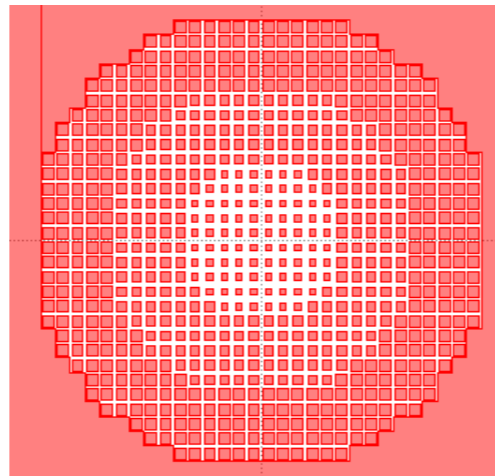
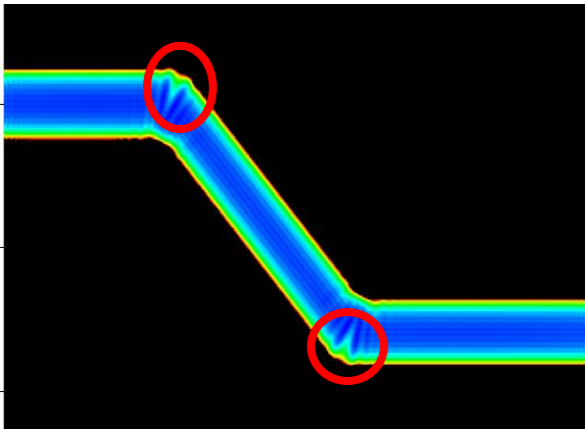


Process window



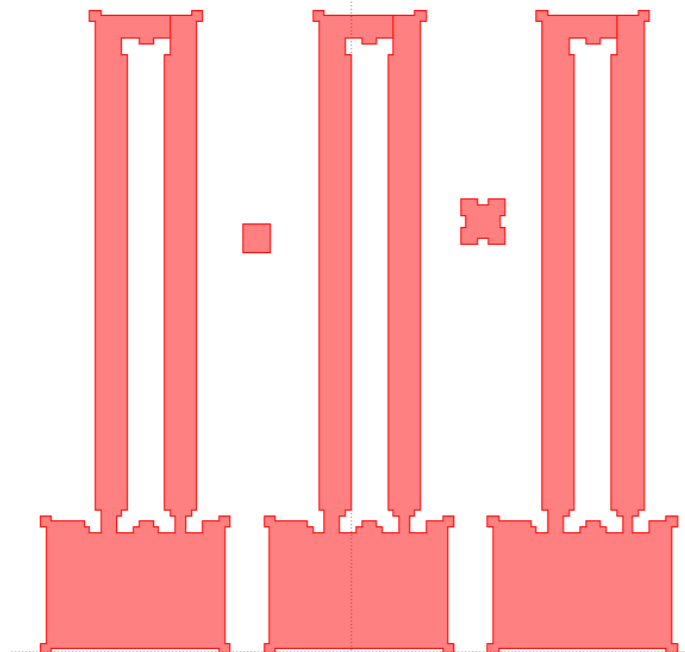
- Proximity Lithography
- 3D Exposure Simulation
- Application Cases
 - Proximity Artifacts Tracking
 - Sidewall Angle Optimization
 - Greyscale Lithography
 - Topography Simulation
 - Resolution Enhancement
- Summary
- Q&A

- Exposure simulation has shown its power in lithography. With a proper model, simulation helps reduction of experimental tryout efficiently. From intensity analysis to resist development, LAB has been used to
 - avoid proximity artifacts
 - optimize resist features, e.g. sidewall angle
 - design greyscale pattern
 - simulate the influence of non-flat substrate
 - enhance the process resolution via OPC

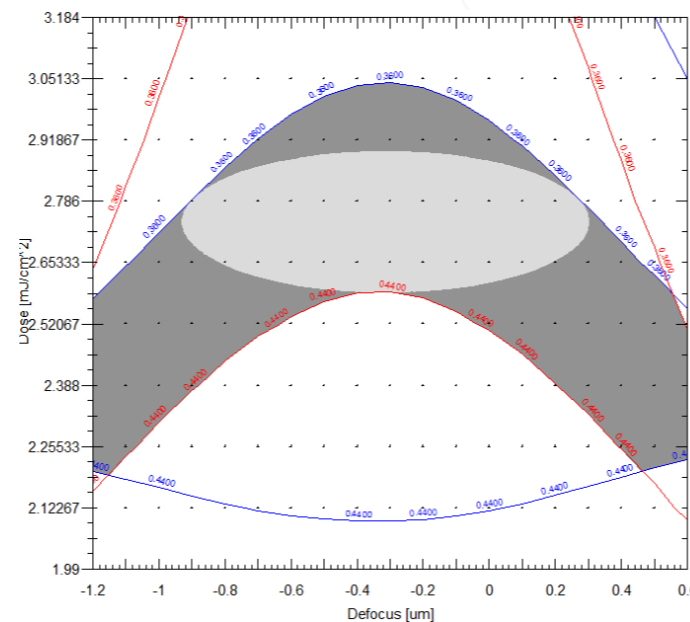


- Exposure simulation is a mandatory tool in projection lithography. LAB, as a simulation tool, can be used for
 - Stack optimization to improve process stability
 - Process feasibility verification
 - Model/Rule based OPC
 - ...

OPC design



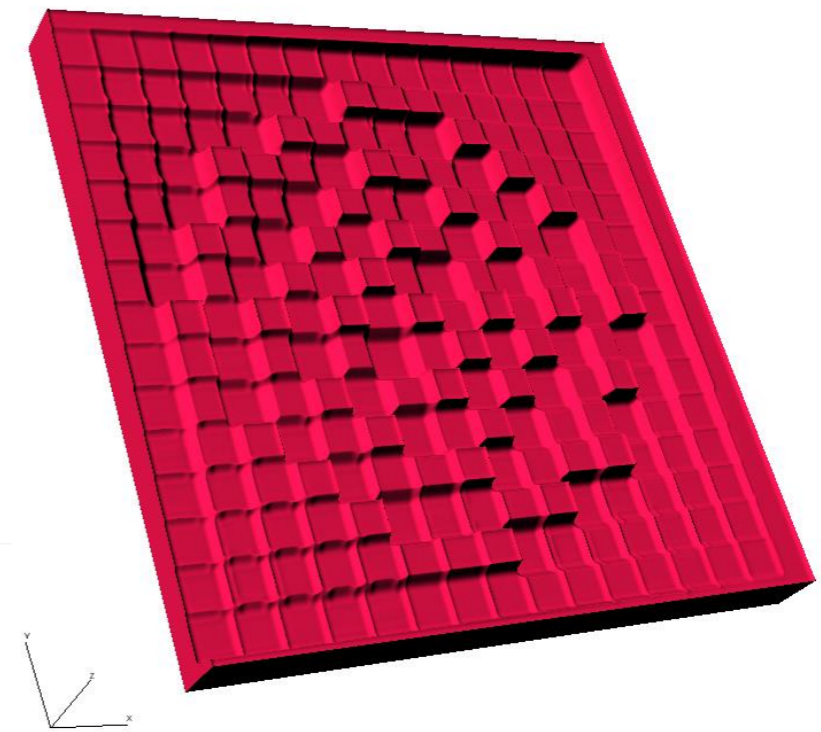
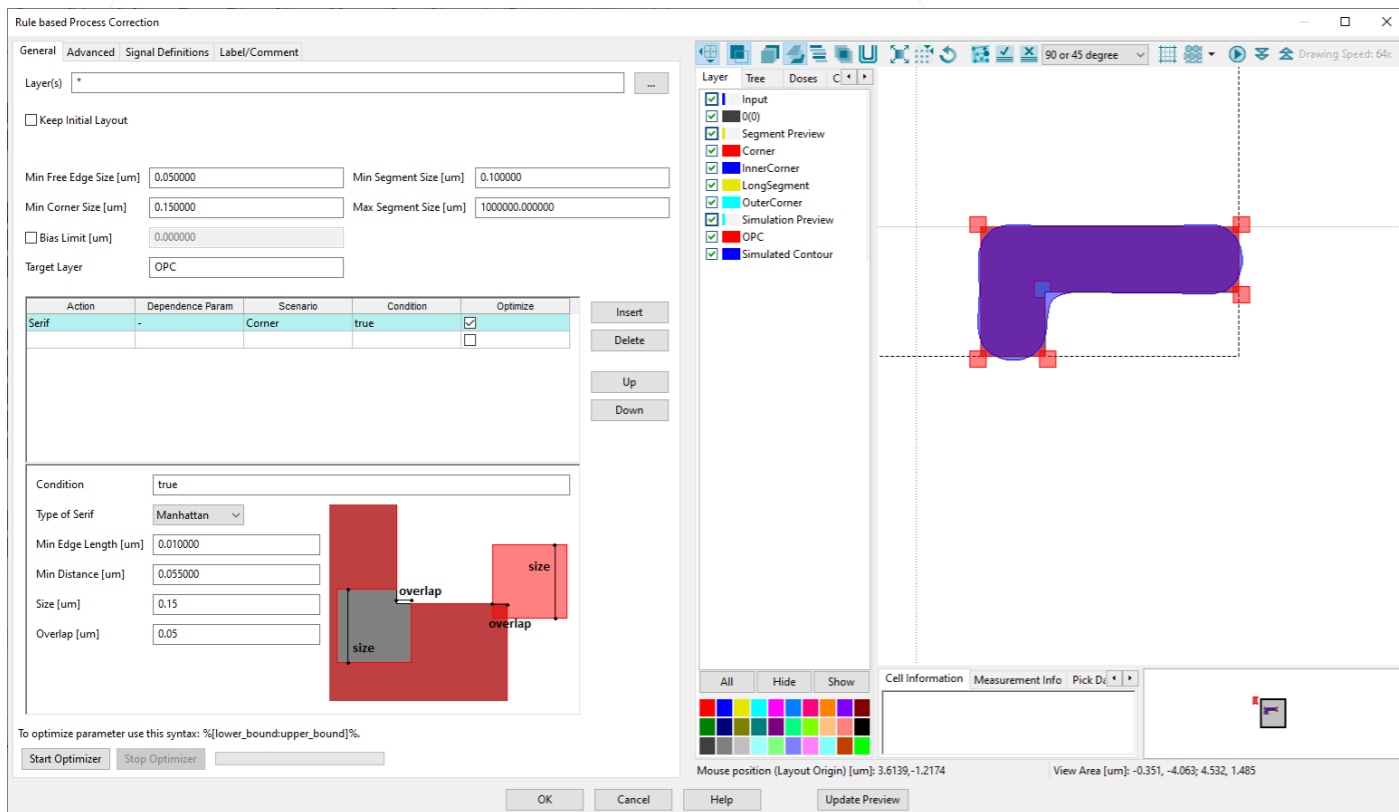
Process window



- Laser lithography is also available in LAB for
 - Process optimization, e.g. OPC design
 - Greyscale structure verification

OPC optimizer

Greyscale structure



- [1] <https://global.canon/en/product/indtech/fpd/spe813.html>
- [2] <https://www.apple.com/>
- [3] <https://www.samsung.com/us/monitors/>
- [4] <https://circuitdigest.com/tutorial/what-is-mems-various-mems-devices-and-applications>
- [5] https://www.suss-microtec.com/technical-publications/wp_simulationforamalith_sussreport_v1_2012_web.pdf
- [6] <https://www.suss.com/de/news/technical-publications/reduction-of-proximity-induced-corner-artifacts-by-simulation-supported-process-optimization>
- [7] Fabrication of tapered edgewall apertures using grayscale lithography, K. S. Kiang, S. Kalsi, etc., 39th International Conference on Micro and Nano Engineering (Sep. 2013).

Thank You!

support@genisys-gmbh.com

Headquarters

GenISys GmbH
Eschenstr. 66
D-82024 Taufkirchen (Munich)
GERMANY

📞 +49-(0)89-3309197-60

📠 +49-(0)89-3309197-61

✉ info@genisys-gmbh.com

USA Office

GenISys Inc.
P.O. Box 410956
San Francisco, CA
94141-0956
USA

📞 +1 (408) 353-3951

✉ usa@genisys-gmbh.com

Japan / Asia Pacific Office

GenISys K.K.
German Industry Park
1-18-2 Hakusan Midori-ku
Yokohama 226-0006
JAPAN

📞 +81 (0)45-530-3306

📠 +81 (0)45-532-6933

✉ apsales@genisys-gmbh.com

